TC358749XBG

(H2C+)

Functional Specification

TOSHIBA

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HISTORY

Revision	Date	Note
Rev 0.72	10/08/13	1. Add 80-pin package, product#749 for HDMI Rx ➔ CSI-2Tx (H2C+) 2. Debug registers 0x6500, 0x6504, 0x6508, 0x650C, 0x6510, 0x6514, 0x6518, 0x651C and 0x6520 all read "0", remove from spec. 3.
Rev 0.73	11/17/2013	1. Updated register fields to remove "??" 2. Typo fixed 3. Removing 0x85A5～0x85AE referring in register bit 0x8520[7] description 4. VPGM and REXT description
Rev 0.74	12/25/2013	0x040C register bit15 correct

REFERENCES

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009”
2. MIPI CSI-2, “MIPI Alliance Specification for Display Serial Interface (CSI-2) Version 1.1 Revision 22 Nov 2011”
3. HDMI, “High-Definition Multimedia Interface Specification Version 1.4b March 4, 2010”
4. I2C bus specification, version 2.1, January 2000, Philips Semiconductor
5. IEC 60958, Digital Audio Interface, First Edition, 1999
6. IEC 61937, Digital audio – Interface for non-linear PCM encoded audio bit streams
7. MIPI SlimBus, “MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus (SLIMbus) Version 1.01.01 – 14 July 2008”

Table of content

Table of Figures

List of Tables

1 Overview

The HDMI-RX to MIPI CSI-2-TX (H2C+) is a bridge device that converts HDMI stream to MIPI CSI-2 while providing de-interlacing and auto-scaling features.

System Overview block diagrams are shown below. TC358749 share the same 80-pin package as that of TC358779.

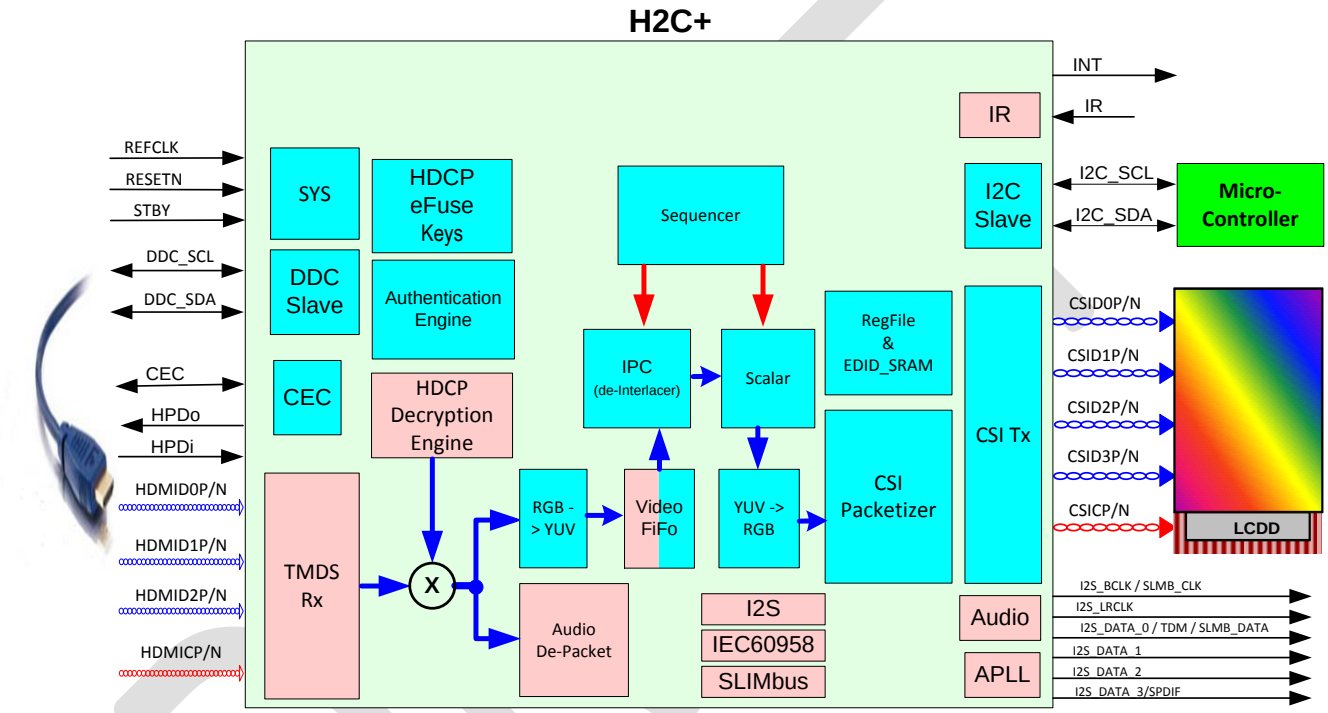


Figure 1-1 TC358749 System Overview

2 Features

Below are the main features supported by TC358749XBG.

HDMI-RX Interface

- ✧ HDMI 1.4b
  - Video Formats Support (Up to 1080P @60fps)
    - ➢ RGB, YCbCr444: 24-bpp @60fps
    - ➢ YCbCr422 24-bpp @60fps
  - Audio Supports
    - ➢ Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
  - 3D Support
  - HDCP1.4a Support
  - EDID Support
    - ➢ Release A, Revision 1 (Feb 9, 2000)
    - ➢ First 128 byte (EDID 1.3 structure)
    - ➢ First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
    - ➢ Embedded 1K-byte SRAM (EDID_SRAM)
  - Maximum HDMI clock speed: 165MHz
- ✧ Does not support Audio Return Path and HDMI Ethernet Channels

CSI-2 TX Interface

- ✧ MIPI CSI-2 compliant (Version 1.1 22 November 2011)
- ✧ Supports up to 4 data lanes @1Gbps/lane
- ✧ Supports video data formats
  - RGB888, RGB666, YCbCr422* 16 & 24bit and YCbCr444

    *: YCbCr422 is not avaialbe if Video Porcessing Module is used.

I2C Slave Interface

- ✧ Support for normal (100KHz), fast mode (400 KHz) and ultra-fast mode (2MHz)
- ✧ Configure all TC358749XBG internal registers
- ✧ Support 2 I2C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)

Audio Output Interface

Any of the four audio interfaces are available: I2S, TDM, SPDIF or SLIMbus (pins are multiplexed)

I2S Audio Interface

- ✧ Up to 4 data lanes for 8-channel data
- ✧ Support Master Clock mode only
- ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
- ✧ Support Left or Right-justify with MSB first
- ✧ Support 32 bit-wide time-slot only
- ✧ Output Audio Over Sampling clock (256fs)
- ✧ Support IEC 60958 & 61937 formats (depending upon HDMI input stream) over I2S
- ✧ Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12MHz

TDM (Time Division Multiplexed) Audio Interface

- ✧ Fixed to 8 channels
- ✧ Support Master Clock mode only
- ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
- ✧ Support 32 bit-wide time slot only
- ✧ Output Audio OverSampling clock (256fs)

SPDIF Audio Interface

- ✧ Supports 2 channels (any 2 of the total 8) (depend on HDMI input stream)
- ✧ Support IEC 60958 & 61937 formats (depending upon HDMI input stream)

SLIMbus Audio Interface

- ✧ Up to 8-channel data (2, 4, 6 or 8)
- ✧ Supports Active Framer (Host) mode as well as active framer outside the chip
- ✧ Active Manager is not supported.
- ✧ Supports Isochronous, Pushed & Pulled protocols
  - Isochronous protocol supported only in Active manager scenario
- ✧ Supports up to 28.8MHz Root Clock Frequency (in Active Framer mode)
- ✧ Supports up to 22 MHz clock frequency on Clk lane (in Active Framer mode)

Video Processing

- ✧ Input formats accepted:
  - RGB or YCbCr422
  - Interlaced or Progressive
  - 2D or 3D
  - Limited to 165 MHz PClk, 640x480, 720x480, 720x576, 1280x720 or 1920x1080 are expected when scalar is used
- ✧ Output formats supported:
  - RGB888, RGB666,YCbCr444 or YCbCr422
  - Interlaced (in case of no video processing) or Progressive
  - 2D or 3D
  - Limited by 4Gbps D-PHY bandwidth, 720x480, 1280x720 or 1920x1080 are expected when scalar is invoked
- ✧ Scaling:
  - Hardware performs scaling automatically based on input and output frame size
    - ➢ HDMI Rx received input frame size and Panel size programmed in registers
    - ➢ Can be overwritten by Software if necessary
  - Horizontal Scaling factors supported:
    - ➢ 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
    - ➢ 2-to-3 and 1-to-3
  - Vertical Scaling factors supported:
    - ➢ 1-to-2, 3-to-2 and 3-to-4
    - ➢ 2-to-1 and 3-to-1
    - ➢ 2-to-3 and 4-to-9
    - ➢ 4-to-5 and 8-to-15
  - Special handling of 3D formats FP, SBS & T&B to avoid boundary artifacts.
- ✧ Color Space Conversion
  - RGB ⇔ YCbCr
  - Two sets of coefficients provided – 1 set for each direction
  - Both color space convertors can be enabled/disabled independent of each other.

InfraRed (IR)

- ✧ Support NEC InfraRed protocol.

System

- ✧ Internal core has two power domains (VDDC1 and VDDC2)
  - VDDC1 is “always-on” power domain
  - VDDC2 can be shut-off during deep sleep mode

Power supply inputs

- ✧ Core and MIPI D-PHY: 1.2V
- ✧ I/O: 1.8V – 3.3V
- ✧ HDMI: 3.3V
- ✧ AVDDPLL: 1.2V
- ✧ Power Consumption during typical operation at room temperature

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDDPLL	Total Power (mW)
		1.2V	1.2V	3.3V	1.8V	1.2V	3.3V	1.2V	1.2V	
1080P @ 60fps	Current (mA)	61.13		0.80	0.89	20.50	72.80	67.82	0.01	421.2
	Power (mW)	73.36		2.65	1.60	24.60	240.25	81.39	0.01	
720p ➔1080p @ 30fps	Current (mA)	170.40		0.80	0.89	20.02	72.66	56.67	1.12	539.23
	Power (mW)	204.48		2.64	1.60	24.02	239.78	68.00	1.34	

Note:

- TC358749XBG does not perform YCbCr ⇔ YUV conversion. In this document YCbCr, HDMI terminology, is used to indicate video color space.

3 External Pins

Following table gives the signals of TC358749XBG and their function.

Table 3-1 TC358749 Pin Name

Group	Pin Name	I/O	Init (O)	Type	Function	Note
System: Reset & Clock (5)	RESETN	I	---	Sch	System reset input, active low	1.8V -3.3V
	REFCLK	I	---	N	Reference clock input (27/26MHz or 42MHz range)	1.8V -3.3V
	TEST	I	---	N	0: Normal mode 1: Test mode	1.8V -3.3V
	STBY	I	---	N	Standby pin, active low	1.8V -3.3V
	INT	O	L	N	Interrupt Output signal – active high (Level) I2C Slv_Addr_Sel at boot-strap	1.8V -3.3V
CSI-2 TX (10)	CSI-2CP	O	H	MIPI-PHY	MIPI-CSI-2 clock positive	1.2V
	CSI-2CN	O	H	MIPI-PHY	MIPI-CSI-2 clock negative	1.2V
	CSI-2D0P	O	H	MIPI-PHY	MIPI-CSI-2 Data 0 positive	1.2V
	CSI-2D0N	O	H	MIPI-PHY	MIPI-CSI-2 Data 0 negative	1.2V
	CSI-2D1P	O	H	MIPI-PHY	MIPI-CSI-2 Data 1 positive	1.2V
	CSI-2D1N	O	H	MIPI-PHY	MIPI-CSI-2 Data 1 negative	1.2V
	CSI-2D2P	O	H	MIPI-PHY	MIPI-CSI-2 Data 2 positive	1.2V
	CSI-2D2N	O	H	MIPI-PHY	MIPI-CSI-2 Data 2 negative	1.2V
	CSI-2D3P	O	H	MIPI-PHY	MIPI-CSI-2 Data 3 positive	1.2V
	CSI-2D3N	O	H	MIPI-PHY	MIPI-CSI-2 Data 3 negative	1.2V
HDMI-RX (8)	HDMICP	I	---	HDMI-PHY	HDMI Clock channel positive	3.3V
	HDMICN	I	---	HDMI-PHY	HDMI Clock channel negative	3.3V
	HDMID0P	I	---	HDMI-PHY	HDMI Data 0 channel positive	3.3V
	HDMID0N	I	---	HDMI-PHY	HDMI Data 0 channel negative	3.3V
	HDMID1P	I	---	HDMI-PHY	HDMI Data 1 channel positive	3.3V
	HDMID1N	I	---	HDMI-PHY	HDMI Data 1 channel negative	3.3V
	HDMID2P	I	---	HDMI-PHY	HDMI Data 2 channel positive	3.3V
	HDMID2N	I	---	HDMI-PHY	HDMI Data 2 channel negative	3.3V
DDC (2)	DDC_SCL	OD	---	FS-SOD	DDC Slave Clock	3.3V (Note1)
	DDC_SDA	OD	---	FS-SOD	DDC Slave data	3.3V (Note1)
CEC	CEC	OD	---	FS-SOD	CEC signal	3.3V
HPD (2)	HPDI	I	---	N	Hot Plug Detect Input	3.3V (Note1)
	HPDO	O	L	N	Hot Plug Detect Output	3.3V
Audio (7)	A_SCK	O	L	N	I2S/TDM Bit/SLIMbus Clock signal	1.8V -3.3V
	A_WFS	O	L	N	I2S Word Clock or TDM Frame Sync signal	1.8V -3.3V
	A_SD[0]	O	L	N	I2S (ch. 0,1)/TDM/SLIMbus data signal	1.8V -3.3V
	A_SD[2:1]	O	LL	N	I2S (ch. 2,3,4,5) data signal	1.8V -3.3V
	A_SD[3]	O	L	N	I2S (ch. 6,7) data/SPDIF signal	1.8V -3.3V
	A_OSCK	O	L	N	Audio Over Sampling Clock	1.8V -3.3V
IR	IR	I	---	Sch	InfraRed signal	1.8V -3.3V
I2C (2)	I2C_SCL	OD	---	FS-SOD	I2C serial clock	1.8V -3.3V
	I2C_SDA	OD	---	FS-SOD	I2C serial data	1.8V -3.3V
APLL (4)	BIASDA	O	L		BIAS signal	
	DAOUT	O	L		Audio PLL clock Reference Output clock	
	PCKIN	I	---		Audio PLL Reference Input clock	
	PFIL	O	L		Audio PLL Low Pass Filter signal	
POWER (11)	VDDC1				VDD for Internal Core (always ON) (1)	1.2V
	VDDC2				VDD for Internal Core (can be powered down) (2)	1.2V
	VDDIO1				VDDIO1 IO power supply (1)	3.3V

Group	Pin Name	I/O	Init (O)	Type	Function	Note
	VDDIO2				VDDIO2 IO power supply (1)	1.8V - 3.3V
	VDD_MIPI				VDD for the MIPI CSI-2 (1)	1.2V
	VDD_PLL11				VDD for PLL11 (1)	1.2V
	AVDD12				HDMI Phy 1.2V power supply (2)	1.2V
	AVDD33				HDMI Phy & APLL 3.3V power supply (2)	3.3V
Ground (25)	VSS				Ground (25)	
Misc	REXT(Note2)				External Reference Resistor	
	VPGM(Note3)				eFuse program power supply	

Total 80 pins

Note1: These IO are 5V tolerant.
Note2: Please conect to AVDD33 with a 2K ohm resistor (± 1%)
Note3: Please tie to ground

Buffer Type Abbreviation:

N:	Normal IO
FS-SOD:	Failed Safe Pseudo open-drain output, Schmidt input
Sch:	Schmidt input buffer
CSI-2-PHY:	front-end analog IO for CSI-2
HDMI-PHY:	front-end analog IO for HDMI

3.1 Pin Summary

Table 3-2 Pin Count Summary – TC358749XBG

Group Name	Pin Count	Notes
SYSTEM	5	
CSI-2 TX	11	Include Power pins
HDMI RX	13	Include Power, External Resistor pins.
DDC	2	
CEC	1	
Audio	7	
I2C	2	
IR	1	
HPD	2	
APLL	4	Audio PLL – Include Power pin
POWER	7	IO, Core, eFuse
GROUND	25	IO, Core, Analog
TOTAL	**80**	

3.2 Pin Layout

Top View (through the die)

A1 AVDD12	A2 REXT	A3 VDDC2	A4 BIASDA	A5 DAOUT	A6 PFIL	A7 VSS	A8 VDD_PLL11	A9 CDSID3N	A10 CDSID3P
B1 AVDD33	B2 VSS	B3 VSS	B4 VSS	B5 VSS	B6 VSS	B7 PCKIN	B8 VSS	B9 CDSID2N	B10 CDSID2P
C1 HDMICP	C2 HDMICN	C3	C4	C5	C6	C7	C8	C9 CDSICN	C10 CDSICP
D1 HDMID0P	D2 HDMID0N	D3	D4 VSS	D5 VSS	D6 VSS	D7 VSS	D8	D9 VSS	D10 VDD_MIPI
E1 HDMID1P	E2 HDMID1N	E3	E4 VSS	E5 VSS	E6 VSS	E7 VSS	E8	E9 CDSID1N	E10 CDSID1P
F1 HDMID2P	F2 HDMID2N	F3	F4 VSS	F5 VSS	F6 VSS	F7 VSS	F8	F9 CDSID0N	F10 CDSID0P
G1 AVDD33	G2 VSS	G3	G4 VPGM	G5 TEST	G6 VSS	G7 VSS	G8	G9 VSS	G10 A_OSCK
H1 AVDD12	H2 CEC	H3	H4	H5	H6	H7	H8	H9 A_SD_0	H10 A_WFS
J1 DDC_SCL	J2 DDC_SDA	J3 HPDO	J4 INT	J5 I2C_SCL	J6 IR	J7 REFCLK	J8 VSS	J9 A_SCK	J10 A_SD_1
K1 VDDC1	K2 VDDIO1	K3 HPDI	K4 STBY	K5 I2C_SDA	K6 RESETN	K7 VDDIO2	K8 A_SD_3	K9 A_SD_2	K10 VDDC2

Figure 3-1 TC358749XBG 80-Pin Layout Package (Top View)

4 Major Functional Blocks

TC358749XBG consists of the following major blocks: HDMI-RX, CSI-2 Tx, RGB2YCbCr & YCbCr2RGB color convertors, De-Interlacer, Scalar, DDC, CEC, I2S (&TDM), SPDIF, SLIMbus, INT and I2C i/f.

DDC, CEC and I2C slave controller are always enabled which are required for configuring the TC358749XBG chip and to wake up TC358749XBG chip.

The following sections describe each block in detail. In addition, there is a section that describes Clock generation block.

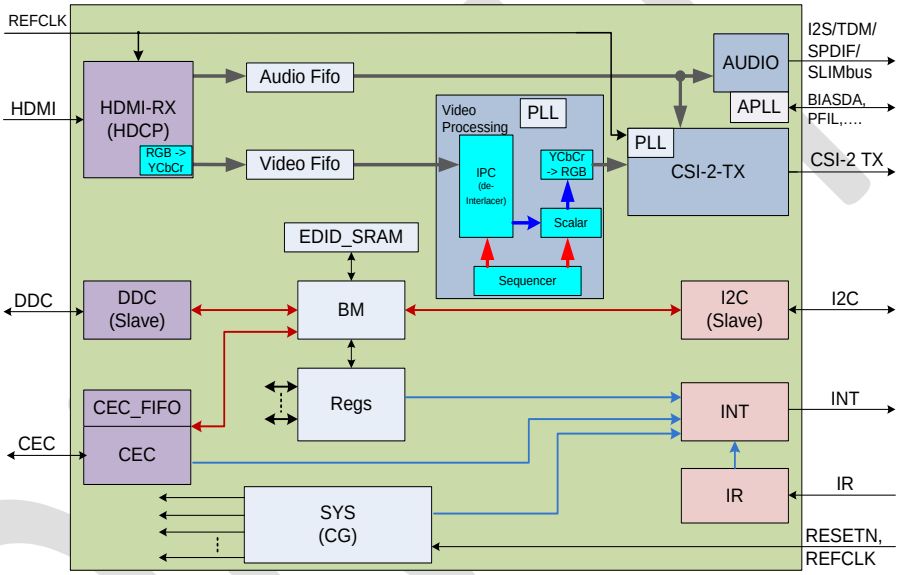


Figure 4-1 Block Diagram of TC358749XBG

4.1 HDMI-RX

Primary features

- HDMI 1.4b
- Video Format support
  - RGB, YcbCr444: 24-bpp @60fps
  - YcbCr422 24-bpp @60fps
- RGB -> YCbCr color space conversion
- Audio
- 3D Support
- Support HDCP 1.3

4.1.1 3D Support

HDMI 3D feature supports the following 3D structures.

Table 4-1 HDMI 3D Structure

Value	Meaning
0000	Frame packing
0001 ~ 0101	Reserved for future use
0110	Top-and-Bottom
0111	Reserved for future use.
1000	Side-by-Side (Half)
1001 ~ 1111	Reserved for future use

4.1.2 Color Space Conversion (RGB to YCbCr)

TC358749XBG provides color space conversion to transfer RGB888 data format to YCbCr444 or YCbCr422. It also provides conversions between YCbCr422 and YCbCr444. The register setting requirement for each conversion is listed below.

4.1.2.1 RGB888 to YCbCr422

0x8574 [3] = 1'b1 (Enable 0x8573 [7])
0x8573 [7] = 1'b1 (YCbCr 422 out selected)
0x8573[6:4] = 3'b100
0x8573[1:0] = 1'b 01 (Use Internal default setting)
0x8576 [7:5] = 3'b 011 or 101 (Output color space setting)
0x0004 [7:6] = 2'b11 (For CSI-2Tx)

4.1.2.2 RGB888 to YCbCr444

0x8574[3] = 1'b1 (Enable 0x8573[7])
0x8573 [7] = 1'b0 (YCbCr444 output selected)
0x8573 [1:0] = 3'b01 (Use Internal default setting)
0x8576 [7:5] = 3'b011 or 101 (Output color space setting)
0x0004 [7:6] = 2'b00 (For CSI-2Tx)

4.1.2.3 YCbCr444 to YCbCr422

0x8574[3] = 1'b1 (Enable 0x8573[7])
0x8573 [7] = 1'b1 (YCbCr 422 output selected)
0x0004 [7:6] = 2'b11 (For CSI-2Tx)

4.1.2.4 YCbCr422 to YCbCr444

0x8574[3] = 1'b1 (Enable 0x8573[7])
0x8573 [7] = 1'b0 (YCbCr 444 output selected)
0x0004 [7:6] = 2'b00 (For CSI-2Tx)

4.2 Video Processing Module

This section describes the video processing pipeline consisting of the following main modules:

- De-Interlacer
- Scalar (Horizontal & Vertical)
- YCbCr to RGB color space conversion

4.2.1 De-Interlacer

De-Interlacer uses 2-D interpolation method to perform noise reduction (NR) and IP conversion.

- Operates in YCbCr color space.
- Output is YcbCr 4:4:4

4.2.2 Scalar

This section describes the Scalar (Horizontal & Vertical) modules. The scalar is supposed to be a smart scalar. Hardware performs scaling automatically based on input frame size and output panel size programmed into registers.

Supported output panel sizes are: 480p (640x480), 720p (1280x720) or 1080p (1920x1080). Possible Input frame sizes to scalar are:

- 640x480p
- 720x480p
- 720x576p
- 1280x720p
- 1920x1080p

Scaling options for both output resolutions are shown in tables below.

Table 4-2 Scaling for 720p Display Resolution

HDMI input	CSI-2 output	Vertical Proc	Horizontal Proc
640x480 P	1280x720 P	2-to-3 scale	1-to-2 scale
720x480 I/P	1280x720 P	2-to-3 scale	9-to-16 scale
720x576 I/P	1280x720 P	4-to-5 scale	9-to-16 scale
1280x720 P	1280x720 P	- pass thru	- pass thru
1920x1080 I/P	1280x720 P	3-to-2 scale	3-to-2 scale

Table 4-3 Scaling for 1080p Display Resolution

HDMI input	CSI-2 output	Vertical Proc	Horizontal Proc
640x480 P	1920x1080 P	4-to-9 scale	1-to-3 scale
720x480 I/P	1920x1080 P	4-to-9 scale	3-to-8 scale
720x576 I/P	1920x1080 P	8-to-15 scale	3-to-8 scale
1280x720 P	1920x1080 P	2-to-3 scale	2-to-3 scale
1920x1080 I/P	1920x1080 P	- pass thru	- pass thru

Table 4-4 Scaling for 480p Display Resolution

HDMI input	CSI-2 output	Vertical Proc	Horizontal Proc
1280x720 P	640x480 P	3-to-2 scale	2-to-1 scale
1920x1080 P	640x480 P	9-to-4 scale	3-to-1 scale

3-D input video can be in SBS (side-by-side or Left-Right), T&B (top & bottom) or FP (frame packing) format.

- For FP format, Video module accepts only progressive video. Interlaced video is not supported. Special handling is needed for scaling of 3D FP format to avoid any artifacts along the last line of top field and first line of bottom field.
- For SBS & T&B formats, both interlaced & progressive video inputs are supported. Special handling is needed for these formats also to avoid any artifacts during scaling along the boundary of two fields in a frame (L & R in SBS or T & B in T&B case).

Table 4-5 3D Scaling for 720p Display Resolution

HDMI input	CSI-2 output	Vertical Proc	Horizontal Proc
1280x720 P FP	1280x720 P FP	- pass thru	- pass thru
1280x720 P SBS (half)	1280x720 P SBS (full)	- pass thru	1-to-2 scale
1280x720 P T&B (half)	1280x720 P T&B (full)	1-to-2 scale	- pass thru
1920x1080 P FP	1280x720 P FP	3-to-2 scale	3-to-2 scale
1920x1080 P SBS (half)	1280x720 P SBS (full)	3-to-2 scale	3-to-4 scale
1920x1080 P T&B (half)	1280x720 P T&B (full)	3-to-4 scale	3-to-2 scale
1920x1080 I SBS (half)	1280x720 P SBS (full)	de-interlace, 3-to-2 scale	3-to-4 scale

Table 4-6 3D Scaling for 1080p Display Resolution

HDMI input	CSI-2 output	Vertical Proc	Horizontal Proc
1920x1080 P FP	1920x1080 P FP *Note	- pass thru	- pass thru
1920x1080 P SBS (half)	1920x1080 P SBS (full) *Note	- pass thru	1-to-2 scale
1920x1080 P T&B (half)	1920x1080 P T&B (full) *Note	1-to-2 scale	- pass thru
1280x720 P FP	1920x1080 P FP *Note	2-to-3 scale	2-to-3 scale

** Note: Frame rate limited to 30fps*

Based on the above tables, only limited scaling factors are required.

- For Horizontal Scaling, ratios required are:
  - 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
  - 2-to-3 and 1-to-3
- For Vertical Scaling, ratios required are:
  - 2-to-1 and 3-to-1
  - 1-to-2, 3-to-2 and 3-to-4

- 2-to-3 and 4-to-9
- 4-to-5 and 8-to-15

Based on the input frame size received from HDMI and the output panel size programmed in the registers, the scaling factor can be determined. Necessary scaling parameters can be chosen accordingly and user does not need to know how to program the scalar.

Option is provided though, to program the parameters manually through software.

4.2.3 Color Space Conversion (YCbCr to RGB)

The color space conversion logic supports a set of 9 programmable coefficient bytes for configuration of YCbCr to RGB color space conversion logic in addition to few other registers to control the output offset. Pls. refer to “YCbCr to RGB” color space conversion registers.

4.3 CSI-2 TX Protocol

In addition to data formats specified by CSI-2 spec, TC358749XBG supports more data formats from HDMI input, including its data island data. Table below shows how TC358749XBG supports/allocates DataType for non-CSI-2 packets.

1. For interlace video, users should program their desired interlace stream DataID in register field PacketID1.VPID0 and PacketID1.VPID1 for top and bottom field, respectively.
2. For CSI-2 specified data formats, DataType follows CSI-2 standard
3. For non-CSI-2 supported YCbCr progressive data formats:
   1. YCbCr444 (8-bit) uses 0x24, which is the same as that of RGB888.
   2. YCbCr422 (12-bit) uses the value programmed in register field PacketID3.VPID2.
   3. The DataType for YCbCr422 (8-bit) depends on register bits set in ConfCtl[YCbCrFmt]
      - ConfCtl[YCbCrFmt] = 2’b10, uses the one in PacketID3.VPID2
      - ConfCtl[YCbCrFmt] = 2’b11, CSI-2 standard specified 0x1E will be used.

Table 4-7 Supported Data Types and Their Data ID fields

DataType ID Register	Description
0x00	Frame Start Code
0x01	Frame End Code
VPID0	For Interlaced frame Top field
VPID1	For Interlaced frame Bottom field
VPID2 (Register PacketID3)	- YCbCr422 12-bit data format packed as CSI-2 RAW12 data format. Data ID is specified in VPID2

DataType ID Register	Description
	- Internal generated pattern, e.g. color bar, uses VPID2 to indicate its data format, which is independent of color format
IFPID	InfoFrame packet. CSI-2 packet ID is defined in PacketID2 register (IFPID parameter)

Note: YCbCr444 8-bit uses the same Data ID as that of RGB888, 0x24

VSYNC, HSYNC and Line# signals in figure below shows conceptual how frame start/end and line start/end related to HSYNC, VSYNC and Line#.

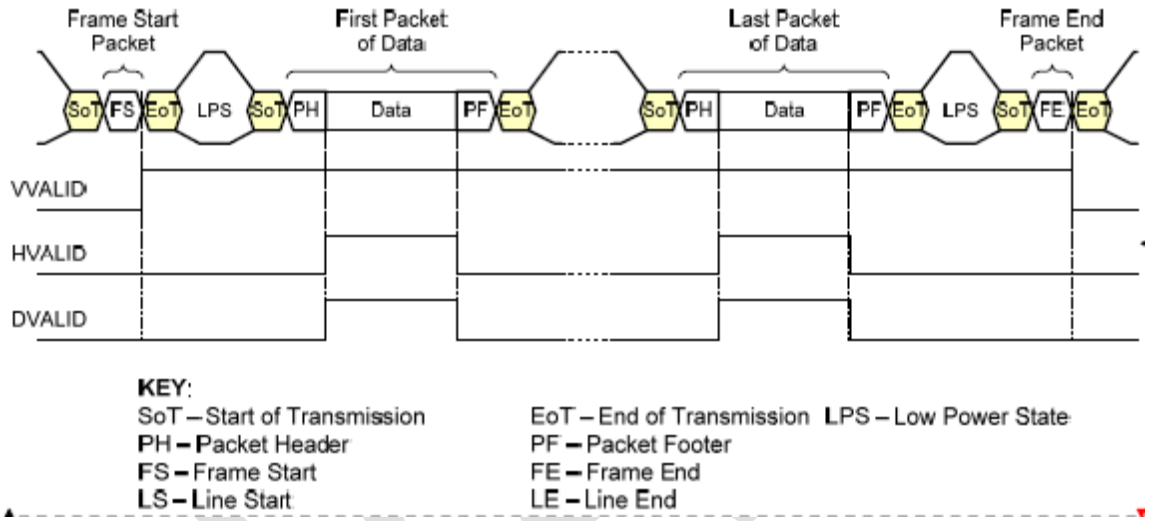


Figure 4-2 Multiple Packet Examle

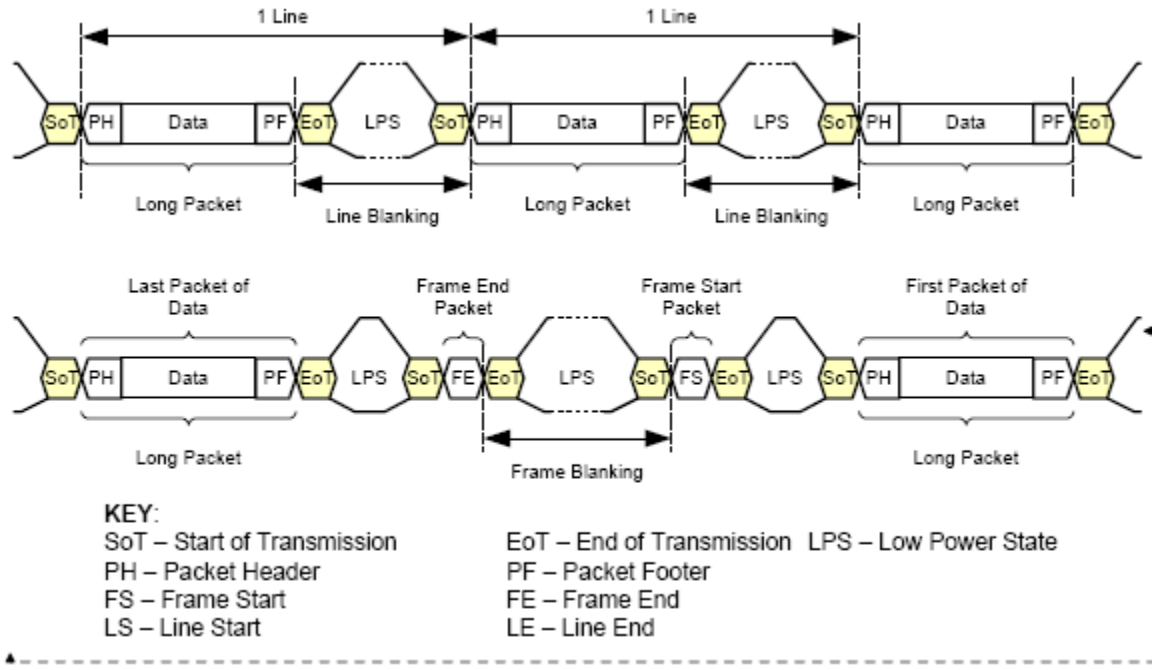


Figure 4-3 Line and Frame Blanking Definitions

CSI-2 terminology:

- Line Blanking Period is the period between the Packet Footer of one long packet and the Packet Header.
- Frame Blanking Period is the period between the Frame End packet in frame N and the Frame Start packet in frame N+1.

The Line Blanking Period is not fixed and may vary in length.

In Serial link, video data is transferred in byte oriented with LSB shifted out first for transmission. The data transmission format of each of video formats in Serial link are shown in Figures below.

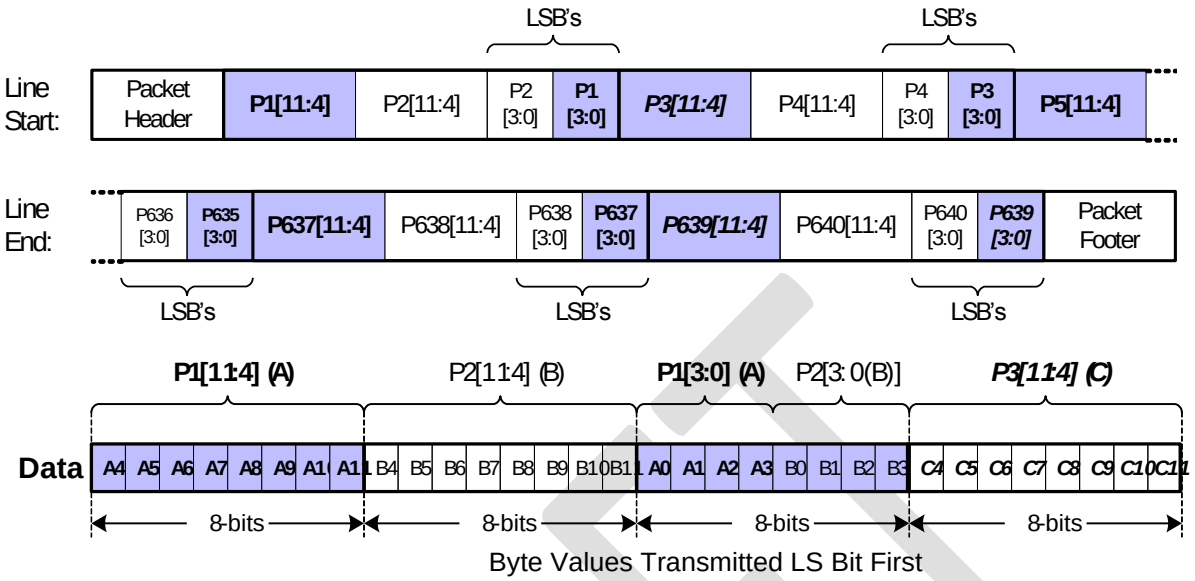


Figure 4-4 RAW12 Data Transmission

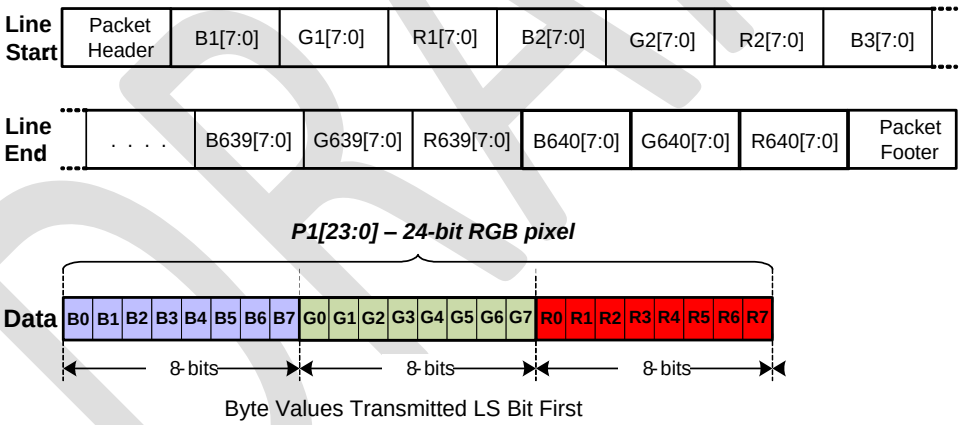


Figure 4-5 RGB888 Data Transmission

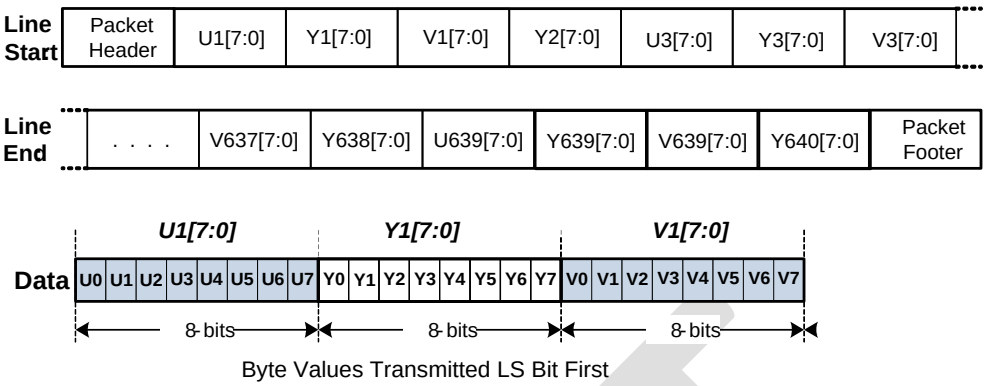


Figure 4-6 YCbCr422 8-bit Data Transmission

All serial byte data will be pack into 32-bit word data before write into the video fifo.

4.3.1 CSI-2 TX Interface Block

The CSI-2 TX consists of CSI-2 D-PHY and Transmit Serial Protocol Layer blocks. The CSI-2 TX supports one clock lane and up to four data lanes which interface with a quad lane Serial Interface.

CSI-2 Tx supports the following video data format

- RGB888 used for RGB, YCbCr444: 24-bpp
- RAW12 used for YCbCr422 12-bit
- YCbCr422 8-bit used for YCbCr 422 12-bit – discard last 4 data bits

A lane merger block in Serial Protocol layer is fetching the 32-bit data from VB module and splitting data to two to four data lanes - CSI-2 D- PHY.

The CSI-2 TX serial video data format is transferred in byte oriented with LSB shifted out first for transmission.

Enable InfoFrame data to send over CSI-2 instead of Host reads Info Frame data over I2C i/f

- All InfoFrame data will send out right after FrameStart packet. Total there are 128 bytes of InfoFrame data

HDMI YCbCr444 data format (used RGB888 data format)

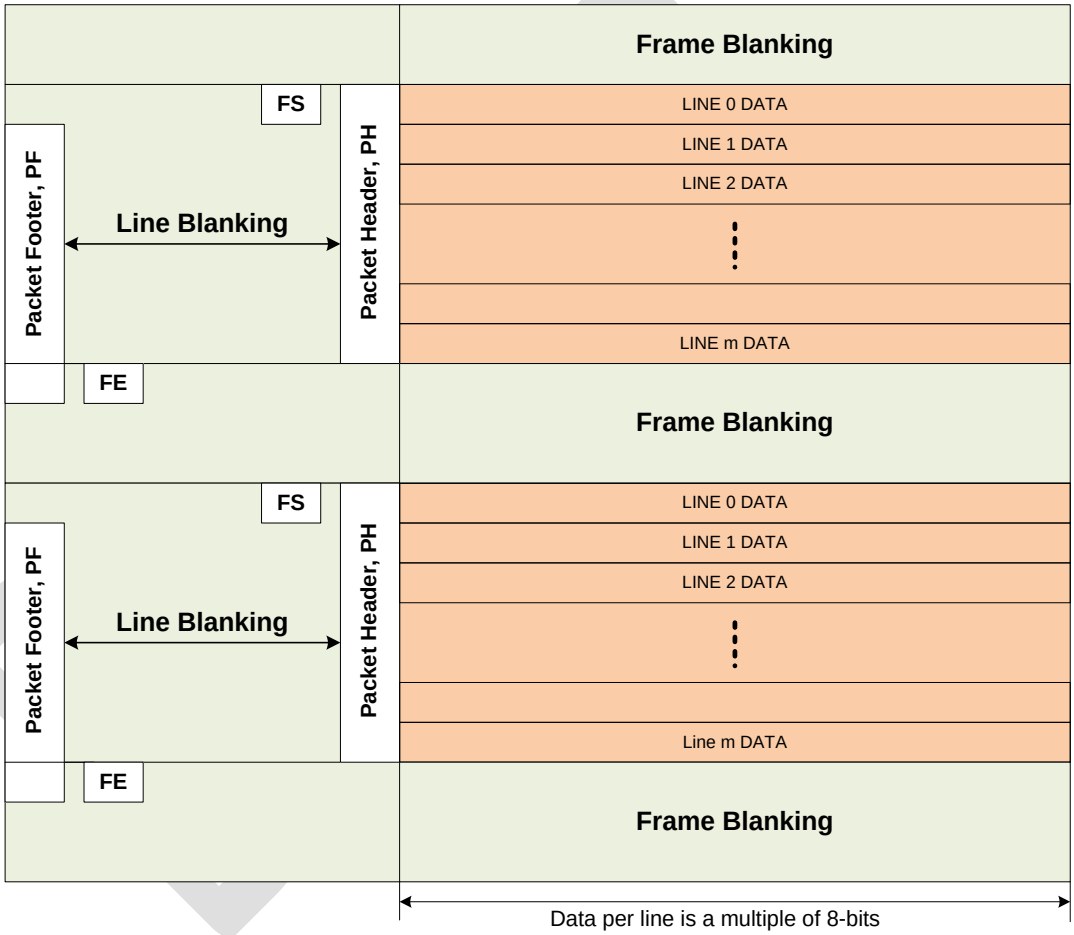
- Y mapped to G
- Cr mapped to R
- Cb mapped to B

HDMI YCbCr422 12-bit data format (used RAW12 data format)

- Cb0 = P1, Cb2 = P5, ….
- Y0 = P2, Y2 = P6,…
- Cr0 = P3 Cr2 = P7,
- Y1 = P4 Y3 = P8

4.3.2 CSI-2 TX Packet Format

The CSI-2 TX packet data formats are showed in Figure 4-9 and Figure 4-10. The Frame format is showed in below Figure.



KEY:
PH – Packet Header
PF – Packet Footer
FS – Frame Start
FE – Frame End

Figure 4-7 Frame Format

4.3.3 Frame Count

Frame count # can be embedded into Frame Start and Frame End packet (in WC field).

Frame count maximum value is defined in FCCtl register.

- When FrCnt = 0, WC field = 0
- When FrCnt = 1, WC field = 1,1,1,1,1,
- When FrCnt = 2, WC field = 1,2,1,2,1,2,.....
- When FrCnt = 3, WC field = 1,2,3,1,2,3,....
- .....

Frame count is increment at every HDMI Vsync.

4.3.4 Checksum Generation

Checksum is calculated over each data packet. The checksum is realized as 16-bit CRC. The generator polynomial is $x^{16} + x^{12} + x^5 + x^0$.

The transmission of the checksum is showed in below Figure.

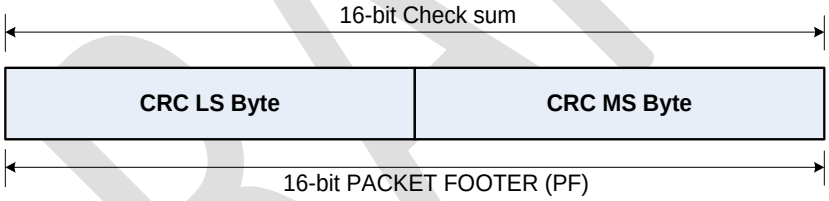


Figure 4-8 Checksum Transmission

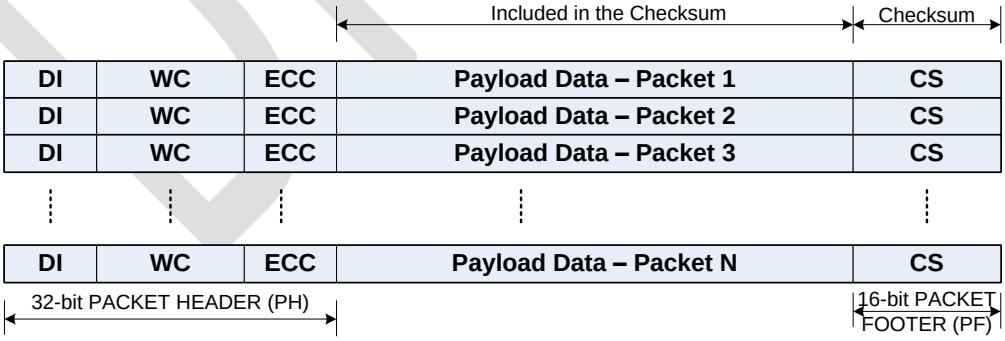


Figure 4-9 Checksum Generation for Packet Data

The 16-bit checksum sequence is transmitted as part of the Packet Footer. When Word Count is zero, the CRC shall be 0xFFFF.

4.3.5 CSI-2 TX One Frame Operation

Below describes the H2C sequence for transmit out the video data onto CSI-2 TX.

1) Enable CSI-2 TX and HDMIRX port.
2) H2C wait for assertion of VSYNC (indicates beginning of frame)
3) H2C wait for the Line buffer reaches the programmable “FIFO Level”.
4) Then transmit “FS” packet for 1st line only
5) Transmit “PH” packet – follow by Line Data until “pixel count” reached
6) Transmit “PF”packet then
    a. Wait Line buffer reaches the programmable FIFO level then loop back to step “5” if Vsync is not active.
    b. If Vsync is active, go to step “7”
7) Transmit “FE” packet, then loop back to step “3”

4.4 CEC Controller

CEC uses a single line to transfer data between TC358749XBG bridge and a HDMI source. Messages are transferred as a single frame, which is built out of a start bit followed by data bits. The bit timing is clearly defined with different timings for the start bit and data bit period. Fixed bit timing is required, because no clock information is transferred over the CEC line.

Each transferred message starts with the transmission of a start bit, which is used to indicate the start of a message and which is also used for arbitration as several device could try to start a transfer. Once arbitration is won, the following information is transmitted in blocks (header block, opcode block and operand block). Each block consists of 8 data bits, one EOM – End Of Message indicator and an acknowledge bit period, where the acknowledge will be used by the addressed device to indicate successful transmission of each block.

TC358749XBG supports the Consumer Electronics Control Protocol as defined in HDMI specification. TC358749XBG offers the physical interface and low level support for data parsing.

4.4.1 Receive Operation Sequence

The following are the sequences for CEC Receive operation

- TC358749XBG collects CEC byte data into Receive FIFO (maximum 16 bytes)
- TC358749XBG asserts INT once it received a valid byte data in the Receive FIFO or after entire message has been received or there is an error condition on the CEC signal protocol.
- TC358749XBG will keep INT at High level until Host complete read out all the Receive data in the FIFO.

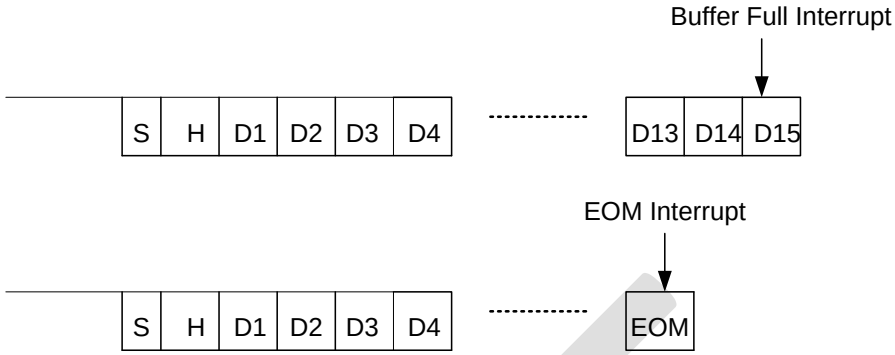


Figure 4-10 CEC reception overview

4.4.1.1 Noise cancellation time

The noise cancellation time is configurable with the CECHNC and CECLNC registers. The CEC line is monitored at each rising edge of the sampling clock. In the case that the CEC line has changed from “1” to “0”, the change is fully recognized if “0”s of the same number as specified in the CECLNC bit are monitored. In the case that the CEC line has changed from ”0” to “1”, the change is fully recognized if “1”s of the same number as specified in the CECHNC bit are sampled.

The following figure illustrates the operation when the noise canceling is configured as CECHNC=10 (3 samplings) and CECLNC =011 (4 samplings). By canceling the noise, a signal “1” shift to “0” after “0” is sampled four times. The signal “0” shifts to “1” after “1” is sampled three times.

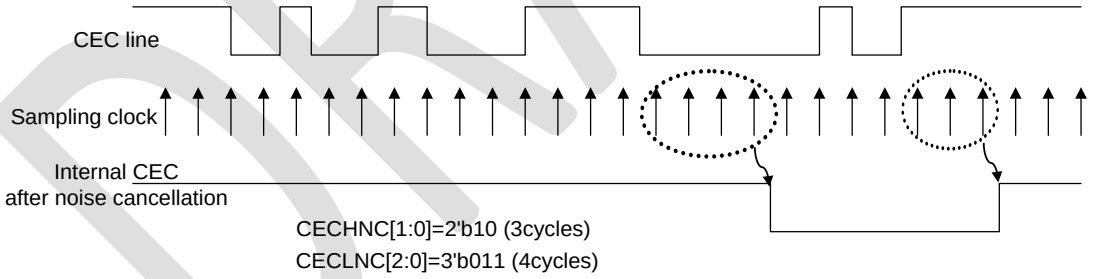


Figure 4-11 CEC noise cancellation example

4.4.1.2 Start bit detection

The following registers are used to detect the start bit of CEC line.

- CECSWAV0 is used to specify the fastest start bit rising timing.
- CECSWAV1 specifies the latest start bit rising timing ((1) in the figure shown below).
- CECSWAV2 is used to specify the minimum number of cycles of a start bit (corresponds to the length of a start bit measured in sampling clock cycles).
- CECSWAV3 specifies the maximum cycle of a start bit ((2) in the figure shown below).

The start bit is considered to be valid if a rising edge during the period (1) and a falling

edge during the period (2) are detected.

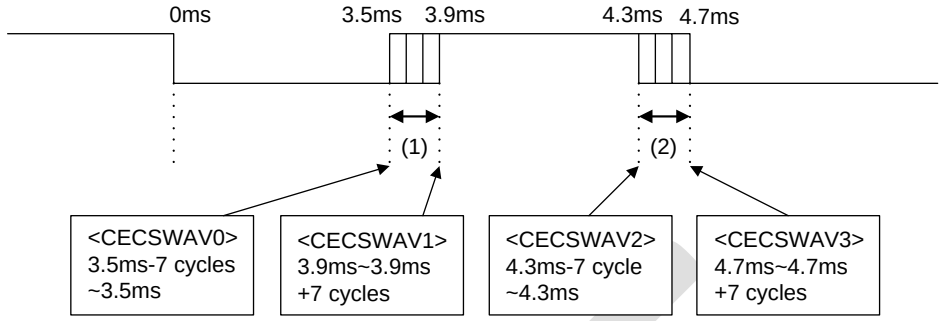


Figure 4-12 CEC start bit detection

4.4.1.3 Waveform Error Detection

The following registers CECWAV0, CECWAV1, CECWAV2, CECWAV3 are used to detect logic transition on CEC line.

A waveform error interrupt is generated if a rising edge is detected during the period (1) or (2) shown below, or if no rising edge is detected in the timing described in (3).

(1) – period between the beginning of a bit and the fastest logical “1” rising timing
(2) – period between the latest logical “1” rising timing and the fastest logical “0” rising timing
(3) – the latest logical “0” rising time

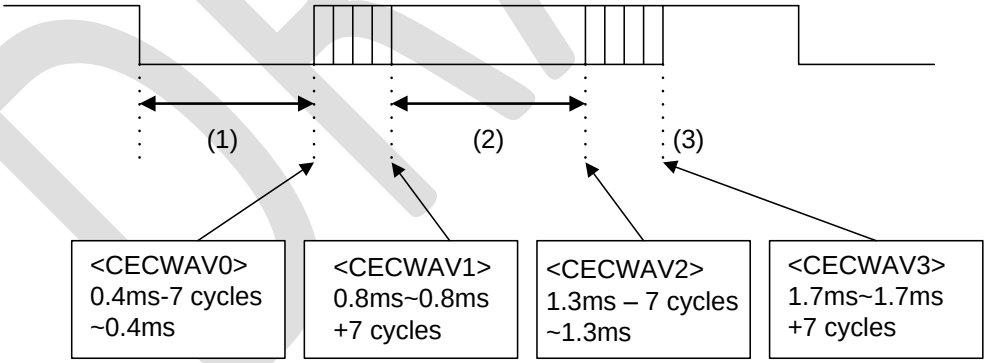


Figure 4-13 waveform error detection

4.4.1.4 Data sampling timing

The figure shown below illustrates a data sampling timing. The CECDAT register specifies the data sampling point per two sampling clock cycles within the range of + or – 6 cycles from the reference point (44pprox.. 1.05 ms).

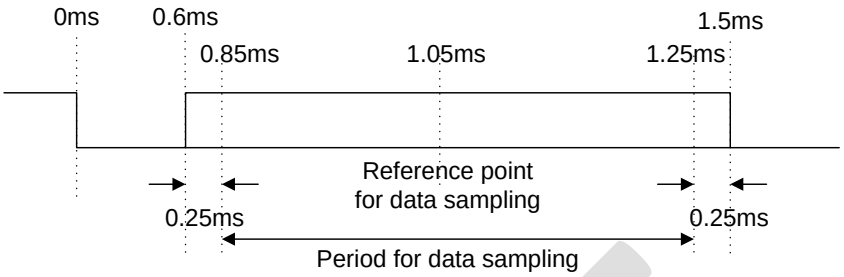


Figure 4-14 sampling time example

4.4.2 Transmit Operation Sequence

The following are the sequence for CEC transmit operation

- Write all transmit CEC byte data into Transmit FIFO (maximum 16 bytes)
- Write "1" to register bit CECTEN[0] to start the operation
- TC358749XBG asserts INT once CEC transmit operation is completed or there is an error condition on the CEC signal protocol.
- Host must read the CEC_Status register to know the status of the transmitting operation and take appropriate action.

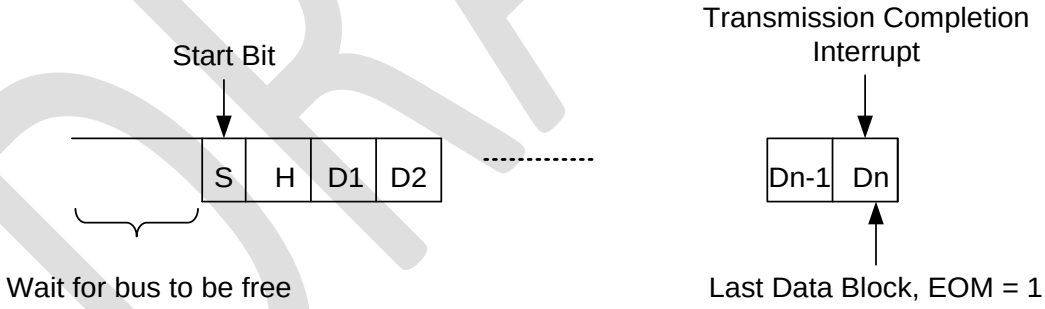


Figure 4-15 CEC transmission example

4.4.2.1 Wait Time for Bus to be Free

The wait time for a bus free check at transmission start is configured with the CECFREE register. It can be specified in a range from 1 to 16 sample clock cycles. Start point to check if a bus is free is the end of final bit. If a bus is free for specified bit cycles of "1", transmission starts.

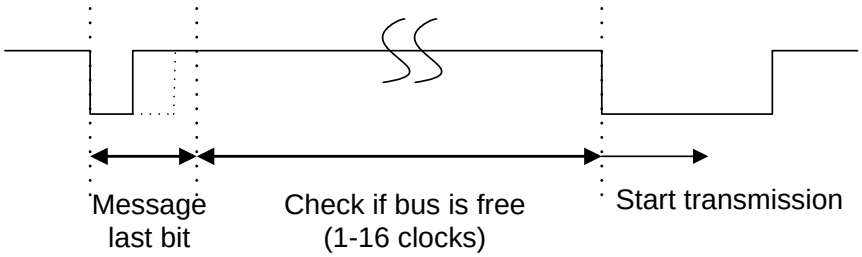


Figure 4-16 Transmission starts

4.4.2.2 Transmission Timing

Timing of the start and data bits can be adjusted with the registers as shown in figure below.

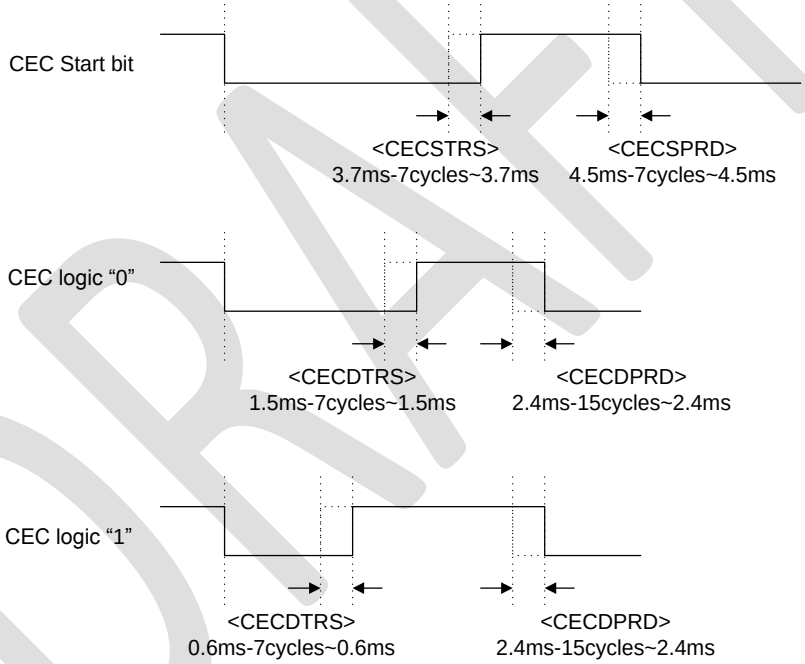


Figure 4-17 Transmission timing

4.4.3 Arbitration lost

An arbitration lost error occurs when CEC module detects “0” during the detection windows as shown in the figure below

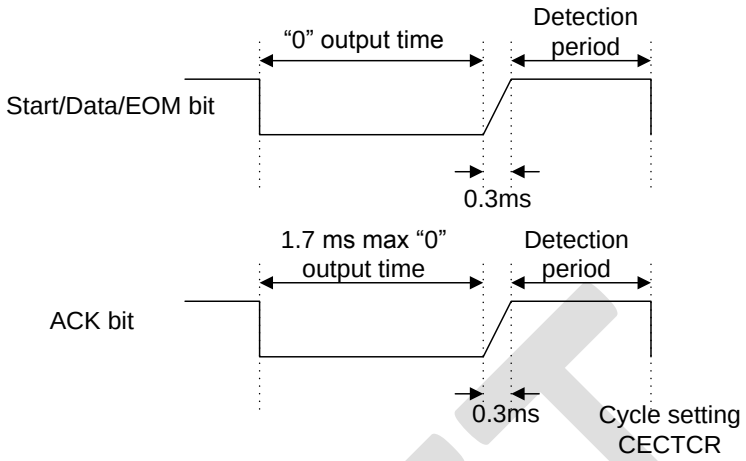


Figure 4-18 Arbitration Error check

4.4.4 Low level functions

In order to ensure transmission on the CEC line, the bridge serves the following low-level functions in accordance to the CEC standard:

- Monitoring of CEC line at all times for any incoming message except when CEC module is off (SET_CEC_ENABLE command).
- Line detection (free/occupied). This function tests the line if it is free to be used.
- Data/Frame parsing. Details of the CEC Frames (header, data blocks, EOM, ACK) will be split and stored.
- Acknowledgment of messages (positive/negative). Success or failure of message transmission will be notified to sender.
- Frame retransmission. Conditional retransmission of lost frames,
- Line error handling. Notification mechanism to inform about spurious pulses on the control signal line.
- Line Arbitration. Collision prevention mechanism.

.

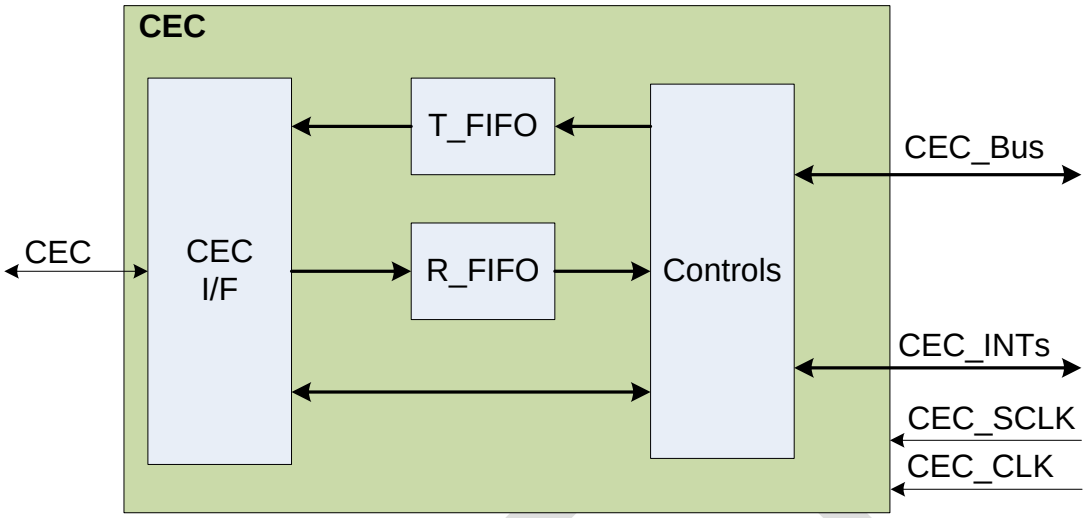


Figure 4-19 CEC Block diagram

4.5 Audio Output Function

TC358749XBG is capable of outputting audio data via I2S I/F, including TDM format, SPDIF I/F or SLIMbus I/F.

The sampling frequency 'f_s' can be 22.05KHz, 24KHz, 32KHz, 44.1KHz, 48KHz, 88.2KHz, 96KHz, 176.4KHz, 192KHz.

TC358749XBG outputs Over-Sampling clock (A_OSCK) with frequency equal to 256f_s when applicable.

4.5.1 I2S Interface

The basic features of the I2S are outlined below:

- Upto 4 output lines (2 Audio channels per line = upto 8 channels)
- Support 16, 18, 20 or 24 bits data
- Support Left or Right-justify with MSB first
- Support 32 bit-wide time slot only.
- Support only Master Clock option

4.5.2 TDM (Time Division Multiplexed) Audio Interface

The basic features of the TDM are outlined below:

- Single output channel
- Support 16, 18, 20 or 24 bits data

- Support up to 8 channels
  - TDM output fixed at 8 channels
  - Fixed at 32 bit-time slot
- Support Master clock only

TDM interface allows multiple channels of data to be transmitted on a single data line. TDM interface is comprised of three signals: a frame synchronization pulse (WFS), serial clock (SCK) and serial audio data (SD).

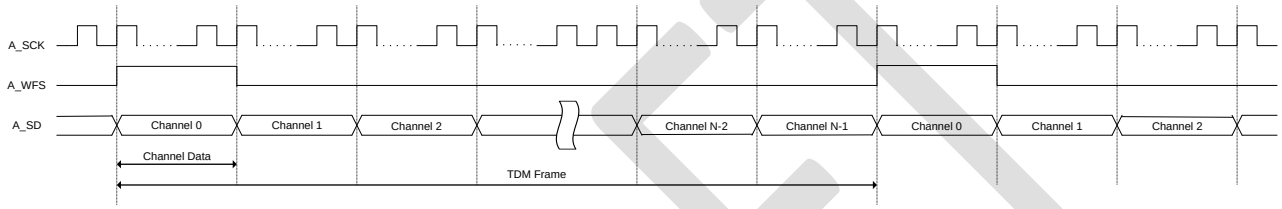


Figure 4-20 I2S N-Channel TDM timing

4.5.3 SPDIF Audio

Incoming HDMI audio stream can support upto 8 channels of audio data. SPDIF supports only 2 channels at any given time. Programming options are available to assign any 2 of the 8 (if available) channels to the SPDIF output channels. Pls. refer 7.9.4.18 AUDIO OUTPUT CHAN_SEL 3 Register (SDO_CHSEL3) (0x8656).

4.5.4 SLIMbus Audio

SLIMbus uses an un-encoded clock line and a NRZI encoded data line for signaling.

- Up to 8-channel data (2, 4, 6 or 8)
- Supports Active Framer (Host) mode as well as active Framer not present mode.
- Active Manager is not supported
- Supports Isochronous, Pushed and Pulled protocols
- Supports up to 28.8MHz Root Clock Frequency (in Active Framer mode)

For Framer, following options are supported:

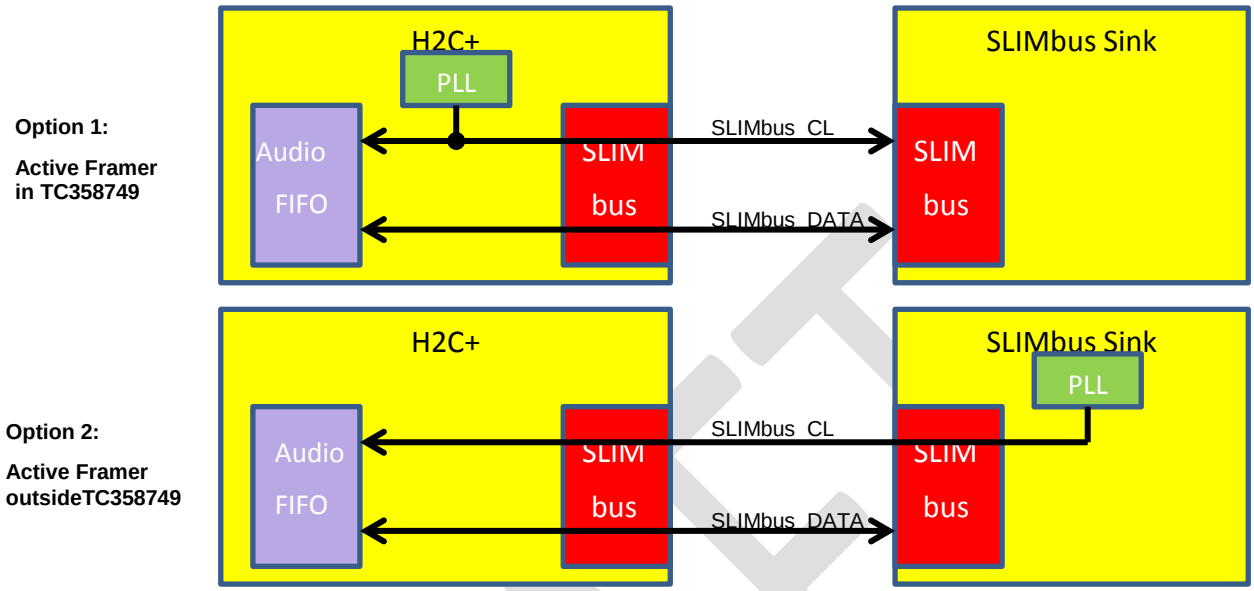


Figure 4-21 Active Framer configurations supported

1. Messages received by TC358749XBG on the SLIMbus causes TC358749XBG to send interrupts to the Host.
2. The interrupts need to be responded to appropriately. As TC358749XBG does not have any intelligence associated.
3. To allow for TC358749XBG to respond properly to SLIMbus messages, following is proposed:
   a. Slow down SLIMbus clock at initialization time.
   b. During actual audio transfer, TC358749XBG can NOT guarantee quick response.
4. **Active Framer Confifuration via SLIMBus is Not recommended.**

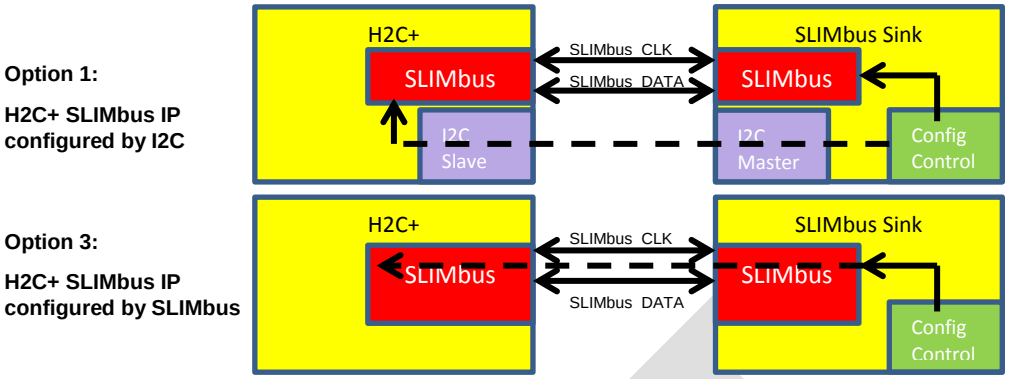


Figure 4-22 Manager Configurations Supported

Figure below provides the basic idea of Frame structure of the SLIMbus transfers.

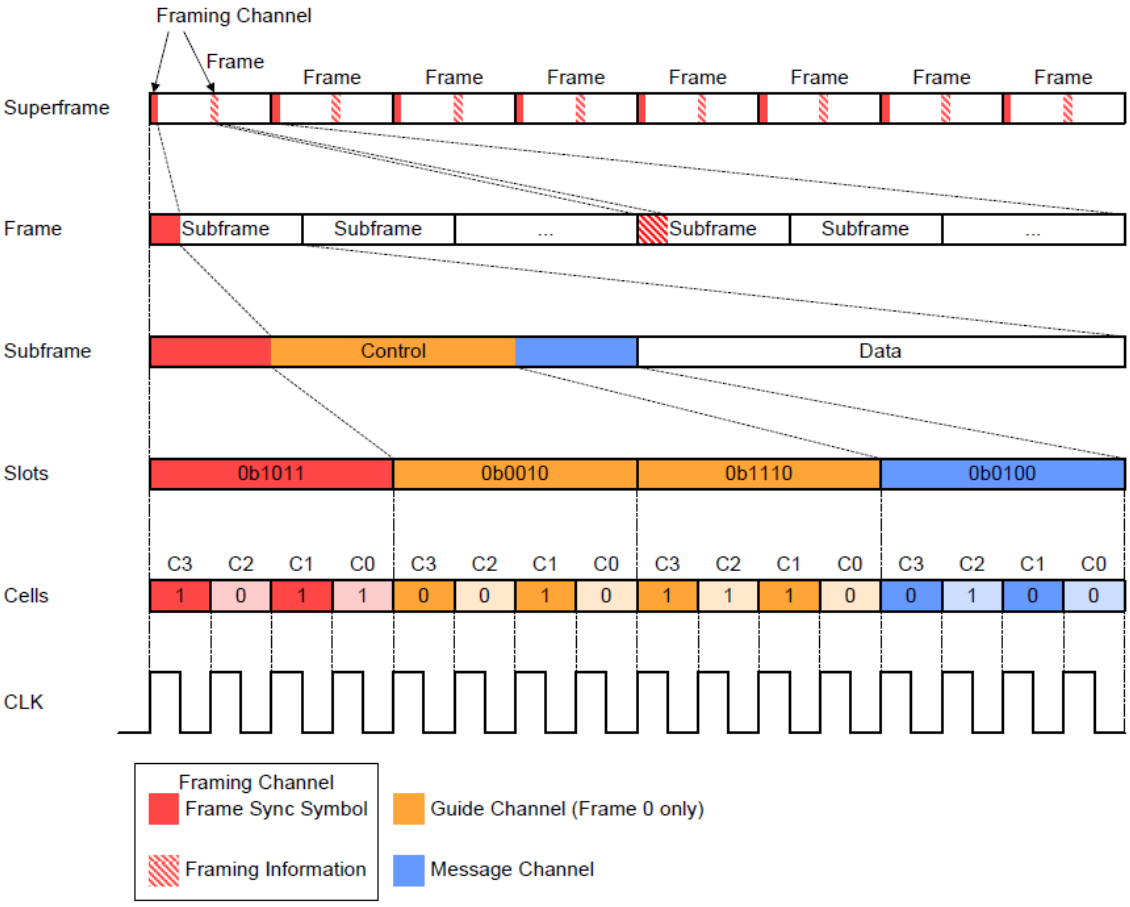


Figure 4-23 Overview of SLIMbus TDM Scheme

Following diagram shows the audio sync pulse generation timing diagram.

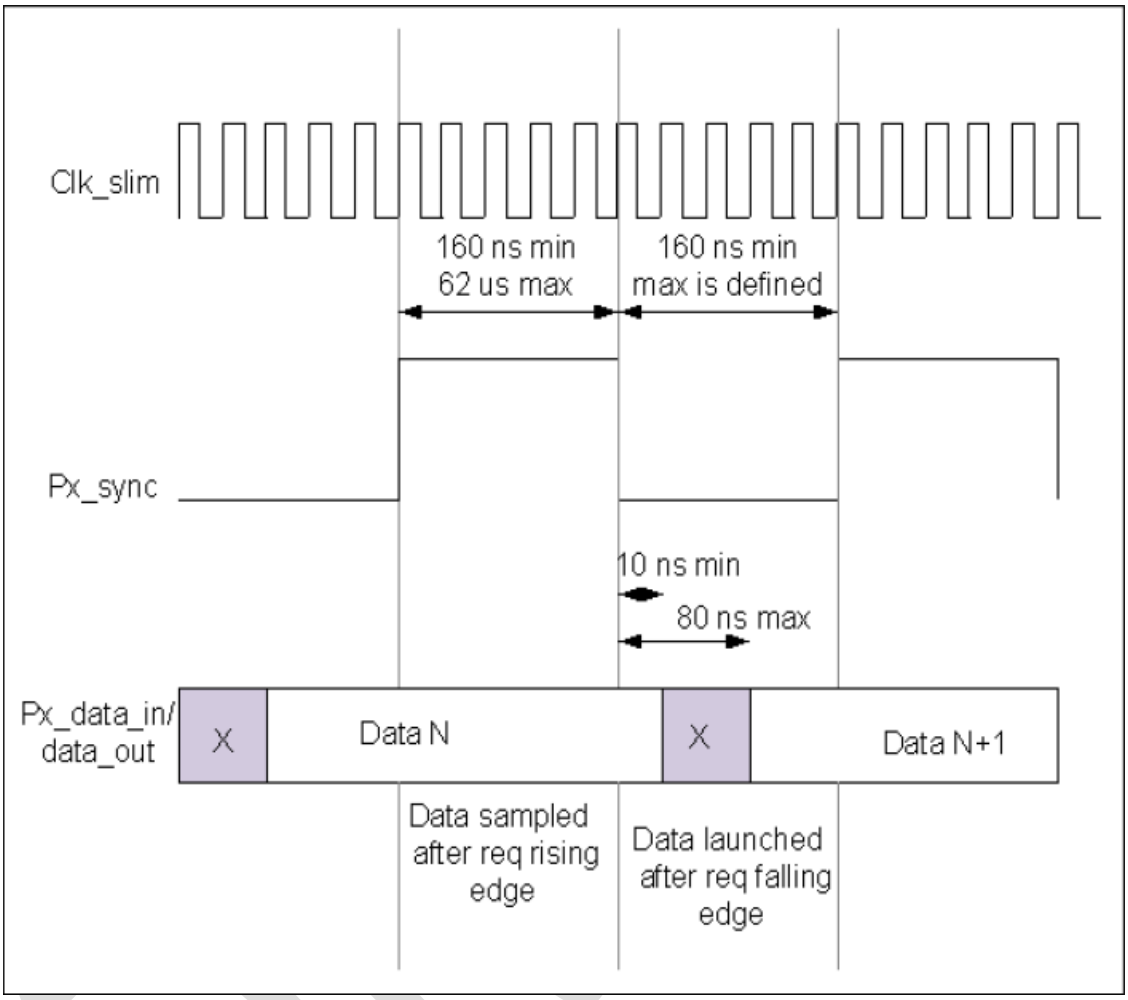


Figure 4-24 Audio Sync Pulse Timing Diagram

Sync_pulse generation starts after activating the channel. Sync_pulse is generated whenever an internal clock counter reaches the period or (period +1) value. Period value is calculated as:

Period = Root Frequency/ Presence Rate

Root Frequency	Period Value in Clock Gear 10		
	Presence Rate 48 KHz Family	Presence Rate 44.1 KHz Family	Presence Rate 8 KHz Family
27.0000	4500	4897	6750
26.0000	4333	4716	6500
25.0000	4166	4535	6250
24.5760	4096	4458	6144
24.0000	4000	4353	6000
22.5792	3763	4096	5644
19.2000	3200	3482	2400
16.8000	2800	3047	4200
15.3600	2560	2786	3840

Figure 4-25 Period Value

Only Isochronous, Pushed and Pulled protocols are supported as defined in SLIMbus specification. Other protocols are not supported.

4.5.4.1 SlimBus Clock Generation

SLIMBus clock can be generated in 3 different ways in TC358749XBG:

- PLL11 based
- HDMI Rx based
- External SLIMbus Active Framer

4.5.4.1.1 SlimBus Clock from PLL11 or External ActiveFramer

PLL11 output always needs to be greater than or equal to 250 MHz (for use in Video IP). A programmable output divider is available outside the PLL11 that can be configured properly (alongwith proper configuration of PLL11) to generate required SLIMbus clock frequencies.

SLIMbus Root Frequency Clock can also be accepted from an external Active Framer (part of external 3rd party SLIMbus module connected to SLIMbus outside of this chip). In order for this mode, the following bits needs to be programmed:

- PLL11_Ctrl1 -> SBRC_Src = 2'b10
- Disable Active Framer in SLIMbus IP

SLIMbus protocols that can be supported in these modes are:

- Pushed
- Pulled

For these protocols, actual root clock frequency can be slightly higher than the required audio data presence rate & the Presence bit is used to inform the availability of audio sample in the frame.

In this scenario, the overall system clock sync is achieved as follows:

- Active Framer (AF) is in AP or AF is in TC358749XBG but internal PLL clock used
- SLIMbus clock lane is slightly over-clocked than required clock rate.
- Data rate is approximation of actual sampling frequency F_s.
- Whenever data is not available from audio FIFO due to rate mismatch, “presence bit, P” is set=0 in SLIMbus packet.
- Clock extracted from HDMI Rx is in sync with HDMI Tx.
- Clock at audio FIFO o/p & on SLIMbus is slightly faster than the HDMI extracted clock.
- Clock in AP is generated based on the nominal F_s information.
- Fine tuning of clock clock in AP is needed to avoid audio buffer under/over flow..

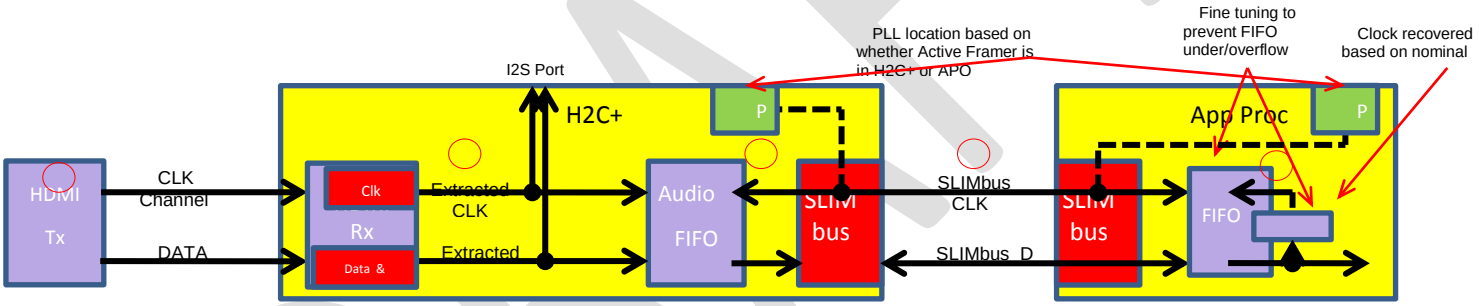


Figure 4-26 SLIMbus Clock source – PLL11 (in TC358749XBG) or outside active framer

4.5.4.1.2 SlimBus Clock from HDMI Rx

SLIMbus Root Frequency Clock can also be generated from the audio over-sampling clock extracted from the HDMI Rx. In order for this mode, the following bits needs to be programmed:

- PLL11_Ctrl1 -> SBRC_Src = 2’b01
- HDMI Rx audio over-sampling clock setting.

This mode supports different sampling rates from 22.05 KHz to 768 KHz based on the programming done to HDMI Audio_Div control registers (0x8666 – 0x866D).

Further, whenever the F_s changes on HDMI side, it is the responsibility of the Host software to broadcast this information well ahead on SLIMbus before actually affecting this change on HDMI side. How to handle this sequence of changing Fs and broadcasting of the message on SLIMbus is beyond the scope of this document. F_s change interrupt can be generated though if set properly.

SLIMbus protocols that can be supported in this mode are:

- Isochronous
- Pushed
- Pulled

In this mode, achieving overall clock sync is inherently built-in as shown in the diagram below.

- Active Framer (AF) is in TC358749XBG & HDMI clock is used
- Clock & Data rate – both accurate multiples of actual sampling frequency F_s.
- Clock extracted from HDMI Rx is in sync with HDMI Tx.
- Clock at all other points is in sync with clock in HDMI Tx.
- Audio data (extracted from HDMI Rx packets) is sent to AP via SLIMbus.
- No chance of drift due to frequency mismatch between HDMI source and SLIMbus sink.

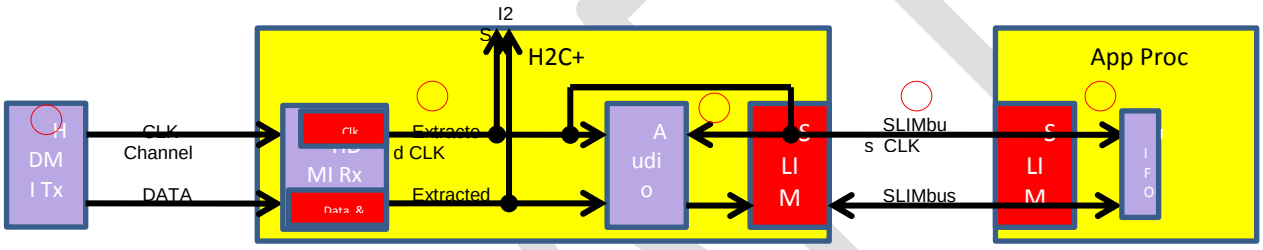


Figure 4-27 SLIMbus Clock source – HDMI Rx extracted clock in TC358749XBG

4.5.4.1.2.1 Fs extraction programming

For proper generation of the Fs (sampling frequency) based on the audio stream input to HDMI Rx, proper dividers need to be programmed in HDMI Rx register space. Below are recommended divider values for different Fs values.

Table 4-8 HDMI F_s v/s divider values

Fs (KHz)	Divider
22.05	1/32
24	1/32
32	1/24
44.1	1/16
48	1/16
88.2	1/8
96	1/8
176.4	1/4
192	1/4
352.8	1/2
384	1/2

Fs (KHz)	Divider
705.6	1/1
768	1/1

4.5.5 IEC 60958/61937 over I2S

The digital audio format streams (IEC 60958 & 61937) can also be sent over the I2S interface.

Traditional I2S audio stream carries only the audio sample data over 1 or more data lines and the clock information is carried on clock line. When sending IEC60958 or IEC 61937 audio streams, the following are differences from normal I2S stream

- Preamble “B” bit information extracted from HDMI & embedded into I2S stream.
- PUCV bits also extracted from HDMI and embedded into the I2S output stream.

Figure below provides the information on the IEC 60958 standard as per the IEC specification.

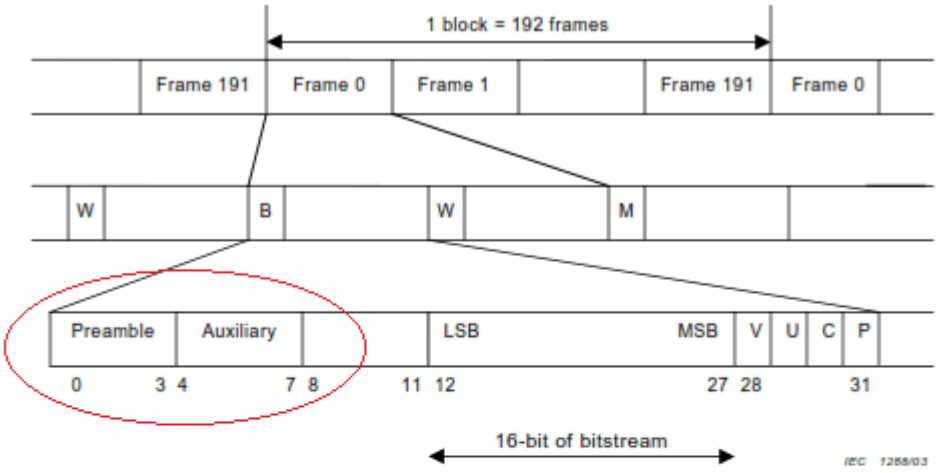


Figure 1 – IEC 60958 interface format

Table 1 – Bit allocation of the IEC 60958 frame

Field	IEC 60958 time-slot	Value
0 – 3	Preamble	IEC 60958 preamble
4 – 7	Auxiliary field	Not used, all "0"
8 – 11	Unused data bits	Not used, all "0"
12 – 27	16-bit data	Sections of the bitstream
28	Validity flag	According to IEC 60958
29	User data	According to IEC 60958
30	Channel status	According to IEC 60958
31	Parity bit	According to IEC 60958

Figure 4-28 IEC 60958 interface format

The diagram below shows how the additional PUCV & Preamble “B” bits will be extracted from HDMI and stuffed into I2S audio frame in this case.

The C, U, V and B bits from the HDMI stream will be included into the 32 bits I2S data format. P bit will be recalculated and included into the 32 bits I2S data format.

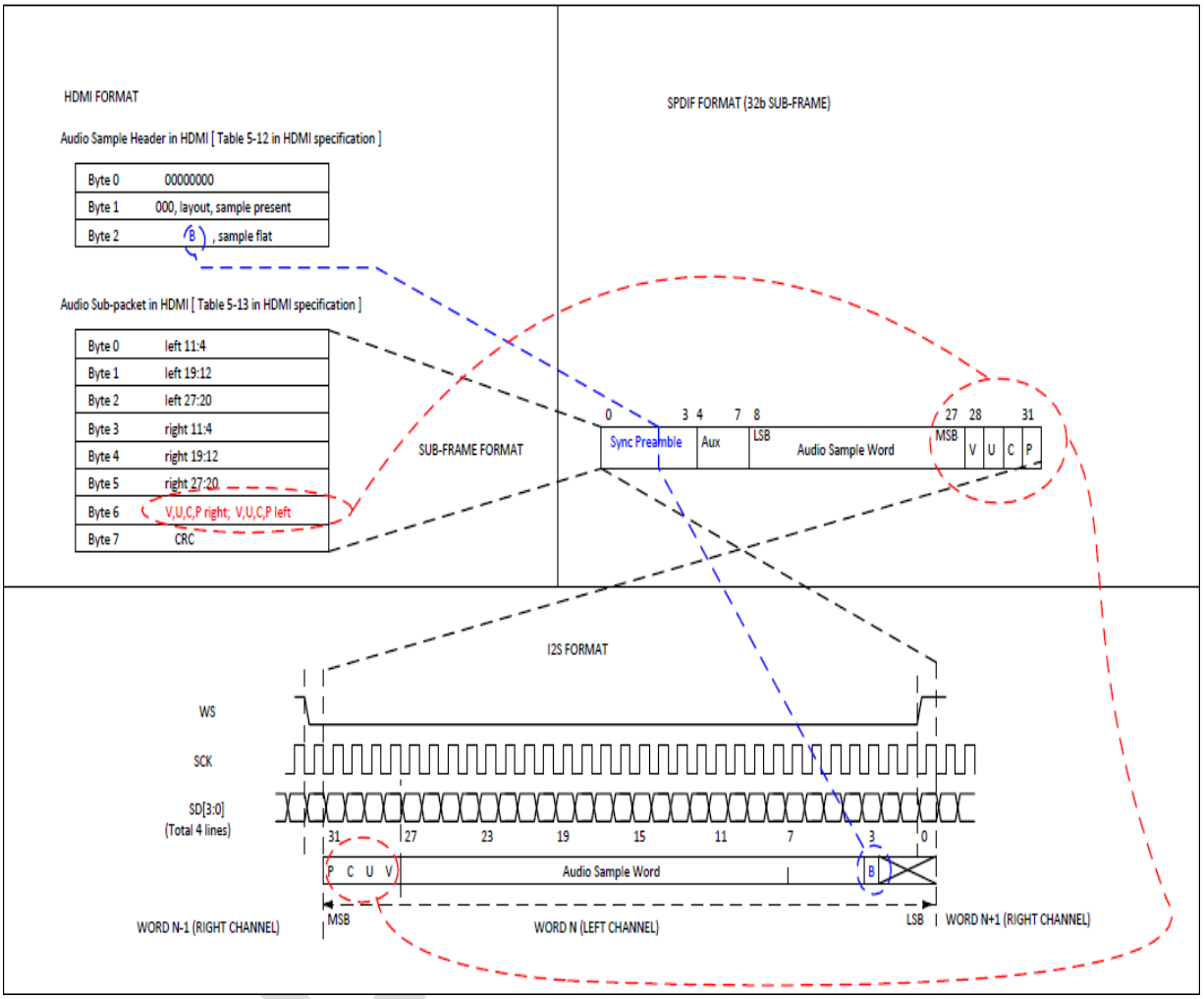


Figure 4-29 Audio_framer for SPDIF over I2S framer

4.5.5.1 HBR Split over I2S

As a special case of I@C60958/61937 over I2S, the HBR audio stream can also be transmitted over the I2S.

But for HBR audio, the F_s is vey high.

- F_s=768kHz: 128fs x 768kHz =98.304MHz
- 764kHz x 64 = 49.152 Mbit/lane.

In some scenarios, the I2S ports of the App Processor may not be able to handle this high data rate. To handle such scenarios, the HBR stream can be splitacross the four (4) I2S data lanes with data rate on each lane reduced by a factor of 4.

Figure below shows this feature conceptually.

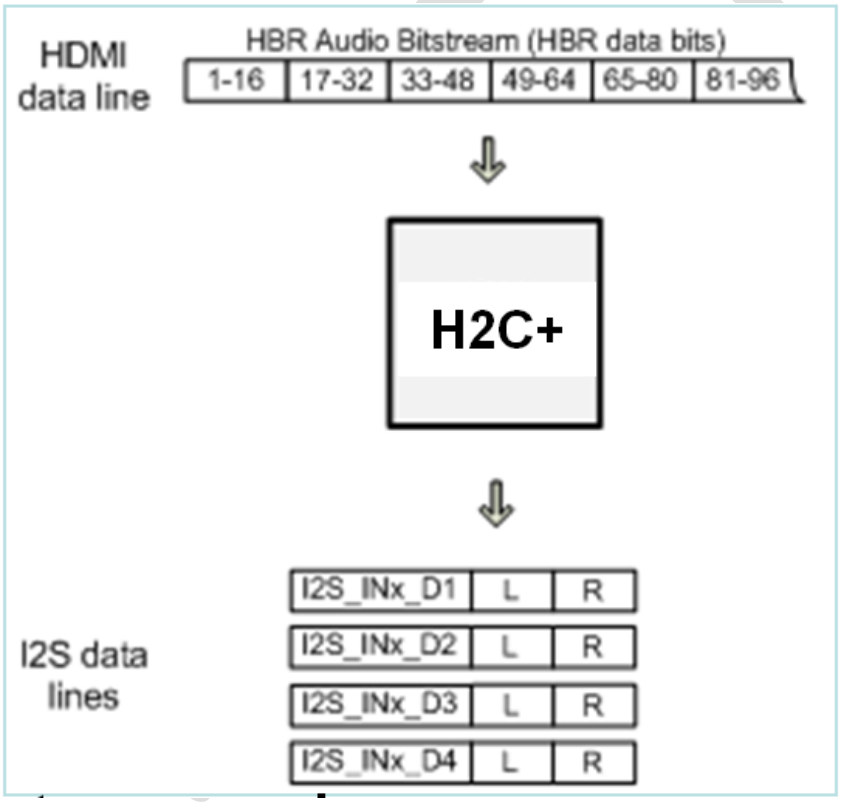


Figure 4-30 HBR Audio stream split over four (4) I2S data lanes

Figure below shows how the HBR audio stream will appear on I2S if not split across four (4) I2S data lanes.

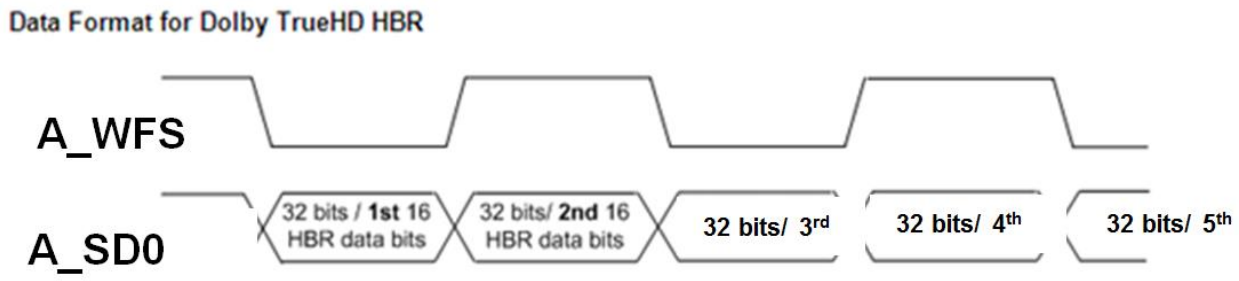


Figure 4-31 HBR Audio stream over 1 I2S lane

Figure below shows how the HBR audio stream will appear on I2S if split across four (4) data lanes.

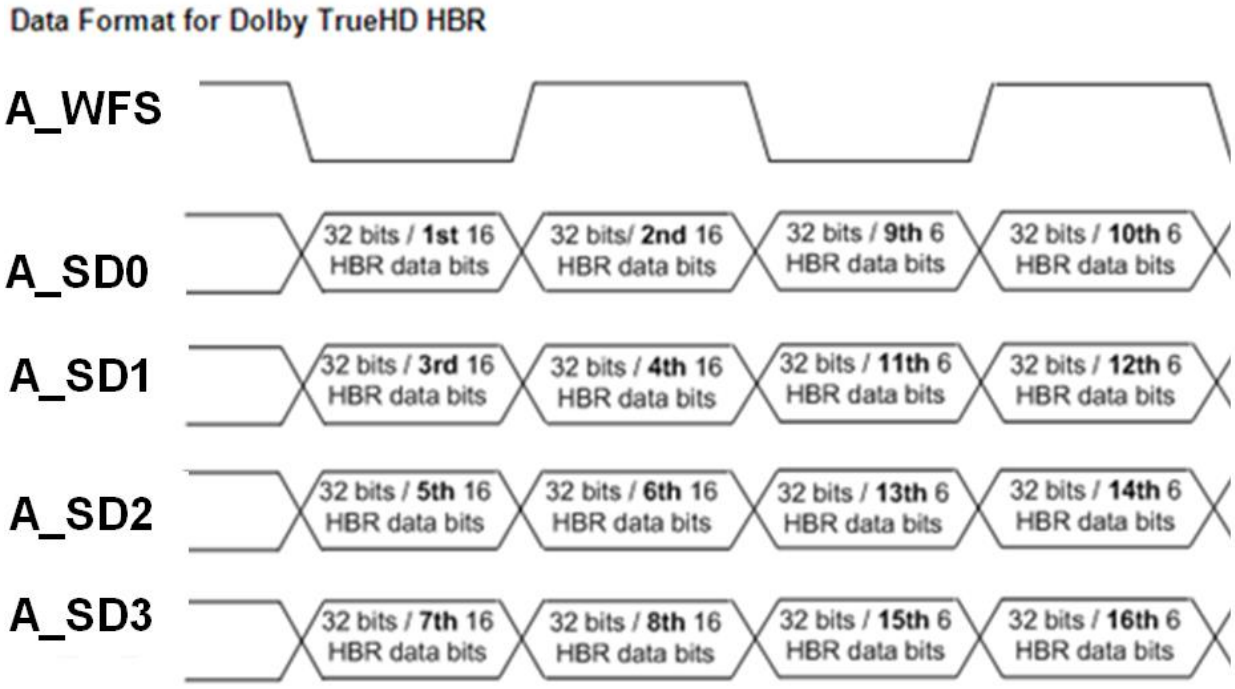


Figure 4-32 HBR Audio stream split over four (4) I2S lanes

4.5.6 Audio PLL LPF Configuration

The Audio PLL external terminal connections used in the Audio clock generation are shown in the Figure below.

In DAOUT output (PLL input), a low pass filter is installed in the LSI external area.

In addition, a low pass filter for cutting unnecessary components in phase comparator output in the PLL is also installed in the LSI external area.

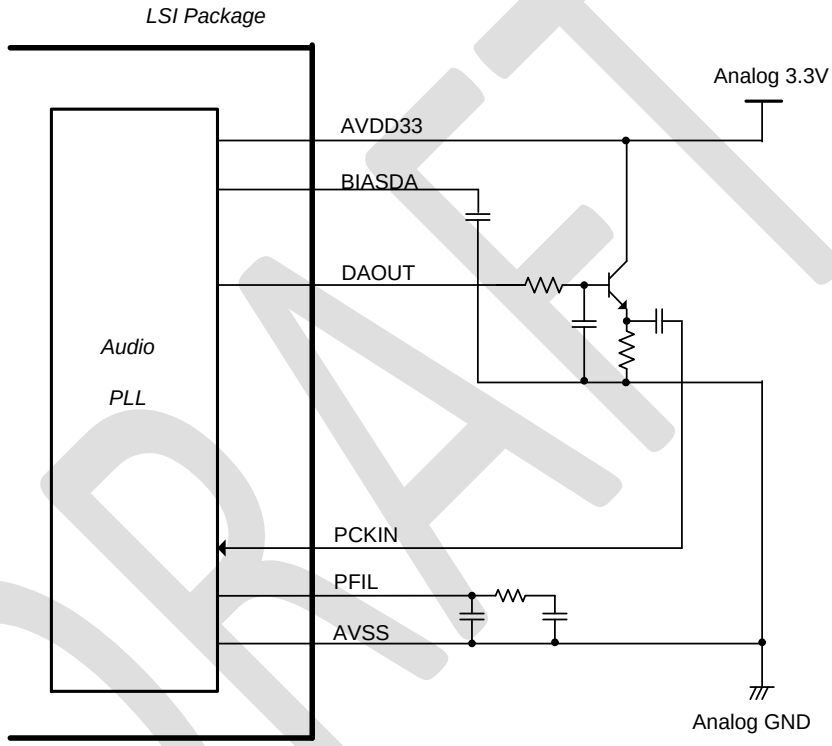


Figure 4-33 Audio Clock External LPF circuit block diagram

4.6 InfraRed (IR) Interface

The basic features of the IR are outlined below:

- Support NEC IR protocol
- Store up to 4 byte IR data
- Interrupt Host when IR address match and detect “end of message” transmission pulse.
- Programmable timing for Leading High time, Leading Low time, Logical “0” H and L time, Logical “1” H and L time.

Supports NEC IR transmission protocol, which uses pulse distance encoding of the message bits. Below figures describes NEC InfraRed protocol.

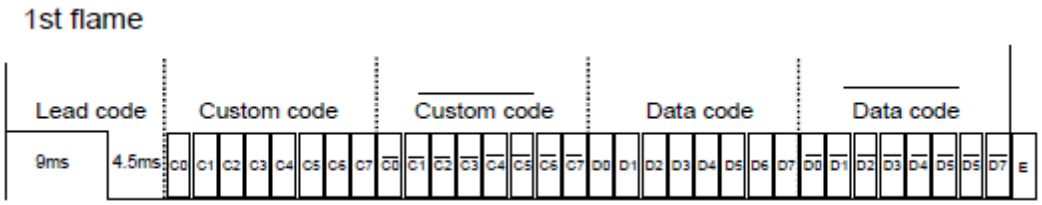


Figure 4-34 NEC Configuration of Frame

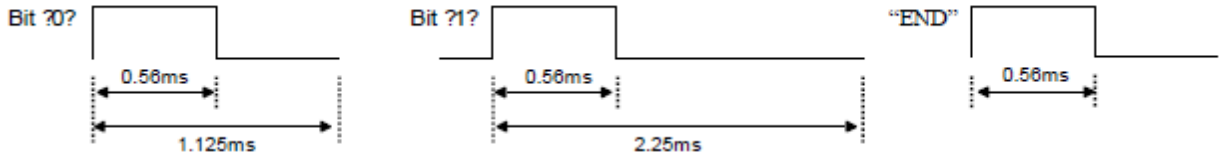


Figure 4-35 NEC Bit Description

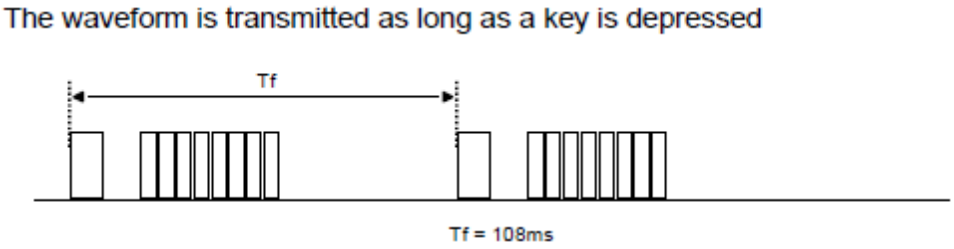


Figure 4-36 NEC Frame Interval (Tf)

4.6.1 Sampling Clock

IR lines are sampled by divide down Refclk (ir_clk).

ir_clk clock is generated from Refclk with divide option for High time and Low time. There are two parameters

1) reg_cech[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
2) reg_cecl[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock .

There are 12-bit counter to count the IR H time and L time with IR sampling clock. Host can configs the appropriate frequency for the IR sampling clock (ir_clk).

4.6.2 Programmable timing

There are four programming timing parameters. IR modules use these timing parameters to detect Lead code, Bit H logic, Bit L logic and “END” flag. Below describes these four timing parameters

1) Detect Lead code when:
    a. H count value is greater than LCHmin parameter (lchmin[11:0]) and smaller than LCHmax parameter (lchmax[11:0]).
    b. L count value is greater than LCLmin parameter (lclmin[11:0]) and smaller than LCLmax parameter (lclmax[11:0]).
2) Detect “L” bit when:
    a. H count value is greater than BitHHmin parameter (bhhmin[11:0]) and smaller than BitHHmax parameter (bhhmax[11:0]).
    b. L count value is greater than BitHLmin parameter (bhlmin[11:0]) and smaller than BitHLmax parameter (bhlmax[11:0]).
3) Detect “H” bit when:
    a. H count value is greater than BitLHmin parameter (blhmin[11:0]) and smaller than BitLHmax parameter (blhmax[11:0]).
    b. L count value is greater than BitLLmin parameter (bllmin[11:0]) and smaller than BitLLmax parameter (bllmax[11:0]).
4) Detect “END” flag when:
    a. After received Lead code – Custom code - /Custom code – Data code - /Data code
    b. H count value is greater than EndHmin parameter (IR_EndHMIN[11:0]) and smaller than EndHmax parameter (IR_EndHMAX[11:0]).

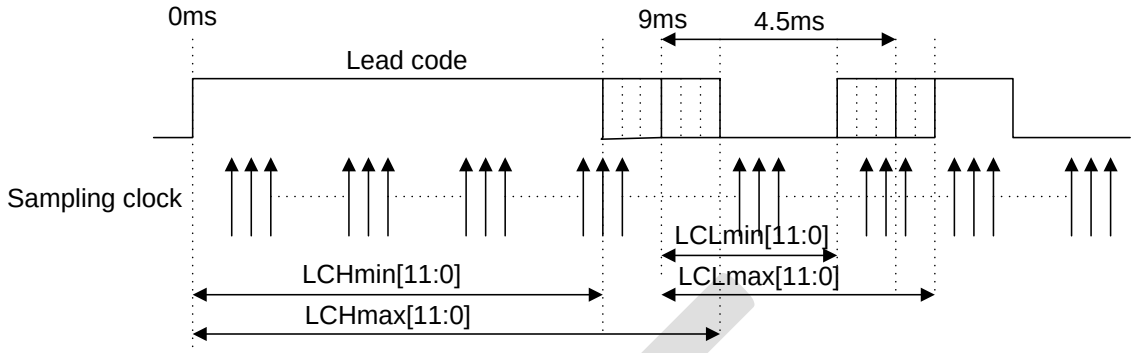


Figure 4-37 Example of Lead Code min/max values for H and L detection

4.6.3 Basic Operation

The following shows the IR sequences:

1) Detect Lead code
2) Receive 8-bit Custom code
3) Receive 8-bit /Custom code
4) IR logic compare the Receive Custom code against the programmable custom code in IR_ccode register. If they are match then IR controller continues to collect the data code. Otherwise it will ignore the IR data.

   (Step 5 – 9 assumes Custom code match)
5) Receive 8-bit Data code
6) Receive 8-bit /Data code
7) Receive “End” code
8) After IR controller receive the “End” code, INT pin will be set (provided that IR_INT is not mask).
   a. If “End” code is not received – entire frame is discarded. Subsequent frame may also be discarded until IR detects the next valid Lead code)
9) Host need to read the 8-bit Data code through the I2C interface. Once the all the IR data code has been read, host needs to clear the interrupt by writing “1” to the respective bit of the Interrupt Status register

Note: IR controller has buffer to store maximum 4 bytes of IR Data code and one 8-bit Custom code (for debugging purpose).

4.7 I2C

TC358749XBG supports an I2C slave function. The I2C module supports the following features:

- Fail safe I2C pad operation
- Up to 400 KHz fast mode operation
- Support special mode – Ultra fast mode 2MHz
- Supports two (2) 7 bit slave addresses recognition:
  - Slave address1 = 7'b000_1111
  - Slave address2 = 7'b001_1111
  - Slave address is selected by boot-strap option using INT pin
- No support for general call address
- Supports 16 bit index value for TC358749XBG I2C slave access

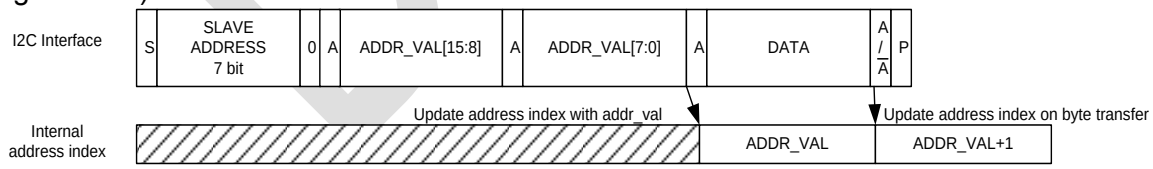
The I2C slave function supports fixed slave address only and does not support general call address. The I2C slave function does not require any programmable configuration parameters.

4.7.1 I2C Slave Address selection through boot-strap

One of the TC358749XBG IO pin has the "Slv_addr_Sel" alternate function at the time of RESET de-assertion. I2C Slave address is selected by boot-strap by latching the value of Slv_addr_Sel input pin at the time of RESET de-assertion. If the value latched is "Low", Slave address1 is selected, otherwise Slave address2 is selected few clocks after the reset de-assertion.

4.7.2 Providing Register Address over I2C Bus

The I2C slave function requires the interfacing I2C master to provide the register address of the TC358749XBG register to be accessed. The I2C slave function loads the first two bytes following a write command as the register address (address index) to be accessed (see Figure 4-38 and Figure 4-39).



S = Start condition
Sr = Repeated start condition
A = Acknowledge
Ã = Not Acknowledge
P = Stop bit

Figure 4-38 Register Write Transfer over I2C Bus

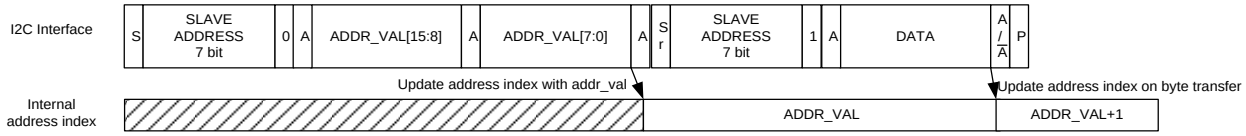


Figure 4-39 Random Register Read Transfer over I2C Bus

I2C slave function supports random write accesses and both random and continuous read accesses (see Figure 4-40).

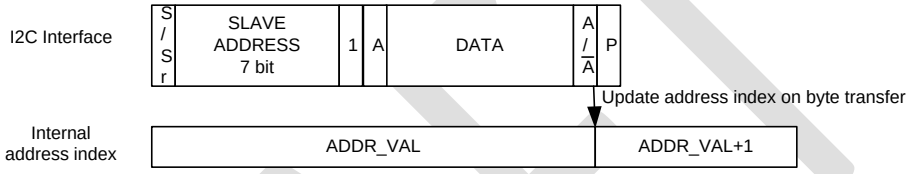


Figure 4-40 Continuous Register Read Transfer over I2C Bus

4.7.3 I2C Write Access Translation

Registers in TC358749XBG are 8, 16 and 32 bit aligned. This implies that I2C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I2C slave controller is always operated in byte boundary. Bus management controller will pack the data to either 8, 16 or 32-bit and write into the register group accordingly.

Note that data transferred on the I2C bus is sent LSB first.

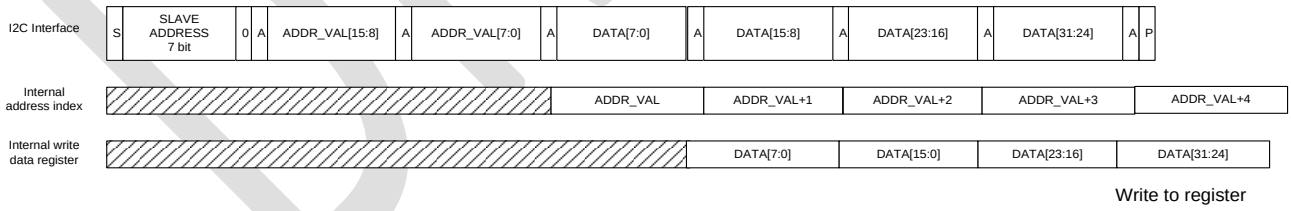


Figure 4-41 I2C Write Transfers Translated to Register Write Accesses

4.7.4 I2C Read Access Translation

Registers in TC358749XBG are 8, 16 and bit aligned. This implies that I2C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I2C

slave controller is always operated in byte boundary. Bus management controller will read the 8, 16 or 32 bit data, un-pack the data to 8-bit and send to I2C controller.

Note that data transferred on the I2C bus is sent LSB first.

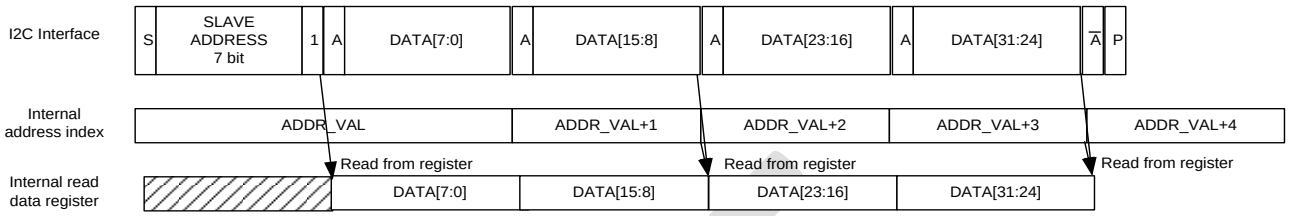


Figure 4-42 I2C Read Transfers to Register Read Accesses

5 Clock and System

TC358749XBG uses totally 4 PLLs.

- One PLL is inside the HDMI Rx and is used to recover the clock from the HDMI stream.
- One PLL is inside the CSI-2 Tx and is used to generate the high speed MIPI Tx clock.
- One PLL is used to generate the high speed 250MHz clock for the Video Processor pipe.
- One PLL is used to generate the Audio over-sampling clock for audio data recovery.

CG supports three powers states RESET, FULLY ACTIVE and SLEEP where clocks are disabled or PLL is disabled to reduce power consumption. SLEEP state is controlled by register bit (reg_sleep).

In RESET: PLL is disabled and no clocks are output. During this state, TC358749XBG will not be able to function.

In FULLY ACTIVE: PLL and TC358749XBG system clock are enabled. Depending on the configuration, I2S controllers may also be enabled.

In SLEEP: PLL is disabled and no clocks are output. During this state,

- Only I2C slave, IR, DDC and CEC interfaces are enabled.
- To wake up TC358749XBG
  - Application processor must wake up TC358749XBG by programming “0” to SLEEP bit (reg_sleep).
  - During Sleep state, TC358749XBG will interrupt Host if either DDC or CEC accesses to TC358749XBG.
- This state may be used by TC358749XBG to safely update PLL parameters when required by the application processor.

CG uses an external input clock REFCLK (27/26MHz or 42 MHz) to generate clocks required by internal controllers.

5.1 Example of PLL Generated Clock Frequency

The possible clock frequencies generated from the PLL are achieved by varying the values in registers PLLFBD and PLLDiv.

*pll_clk = RefClk * [(FBD + 1)/ (PRD + 1)] * [1 / (2^FRS)]*

Table 5-1 provides possible frequencies that may be used in TC358749XBG.

Table 5-1 Possible PLL parameters

Reference clock (MHz)	FBD	PRD	FRS	pll_clk (MHz)
26	255	7	1	416.00
	319	5	2	346.67
	319	6	2	297.14
	319	7	2	260.00

5.2 Output Clocks Generation

SYS_DIV:

sys_clk clock is same as CSI-2 TX Byte clock.

CEC_DIV:

cec_clk clock is generated from Refclk with divide option for High time and Low time. There are two parameters

1. reg_CecHclk[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
2. reg_CecLclk[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock .

IR_DIV:

ir_clk clock is generated from Refclk with divide option for High time and Low time. There are two parameters

1. reg_IrHclk[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
2. reg_IrLclk[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock.

PPI_CLK:

Pixel clock is generated from the HDMI Rx IP based on the clock extracted from the HDMI PHY using the HDMI PHY PLL.

CSI-2CLK:

CSI-2CLK is the CSI-2 Tx clock generated by the CSI-2 Tx PLL and is used for reading data from the final video and audio buffers and for handling the data through the CSI-2 Tx stage.

CLK_266M:

Clk_266M high speed clock is generated from the Refclk using the PLL.

Table 5-2 Controllers' Operating Frequency

Controllers	Operating Frequency		Source
	min (MHz)	max (MHz)	
VIP	---	250	CLK266M
HDMI-RX	---	165	TDM clock
CSI-2-TX	---	125	CSI-2-TX byte clock
af and vf controller	---	125	CSI-2-TX byte clock
DDC, CEC, EDID_SRAM, REG, BM, I2C and INT	27/26	42	RefClk

5.3 Clock Diagram

The following diagram shows the clocks of the overall chip.

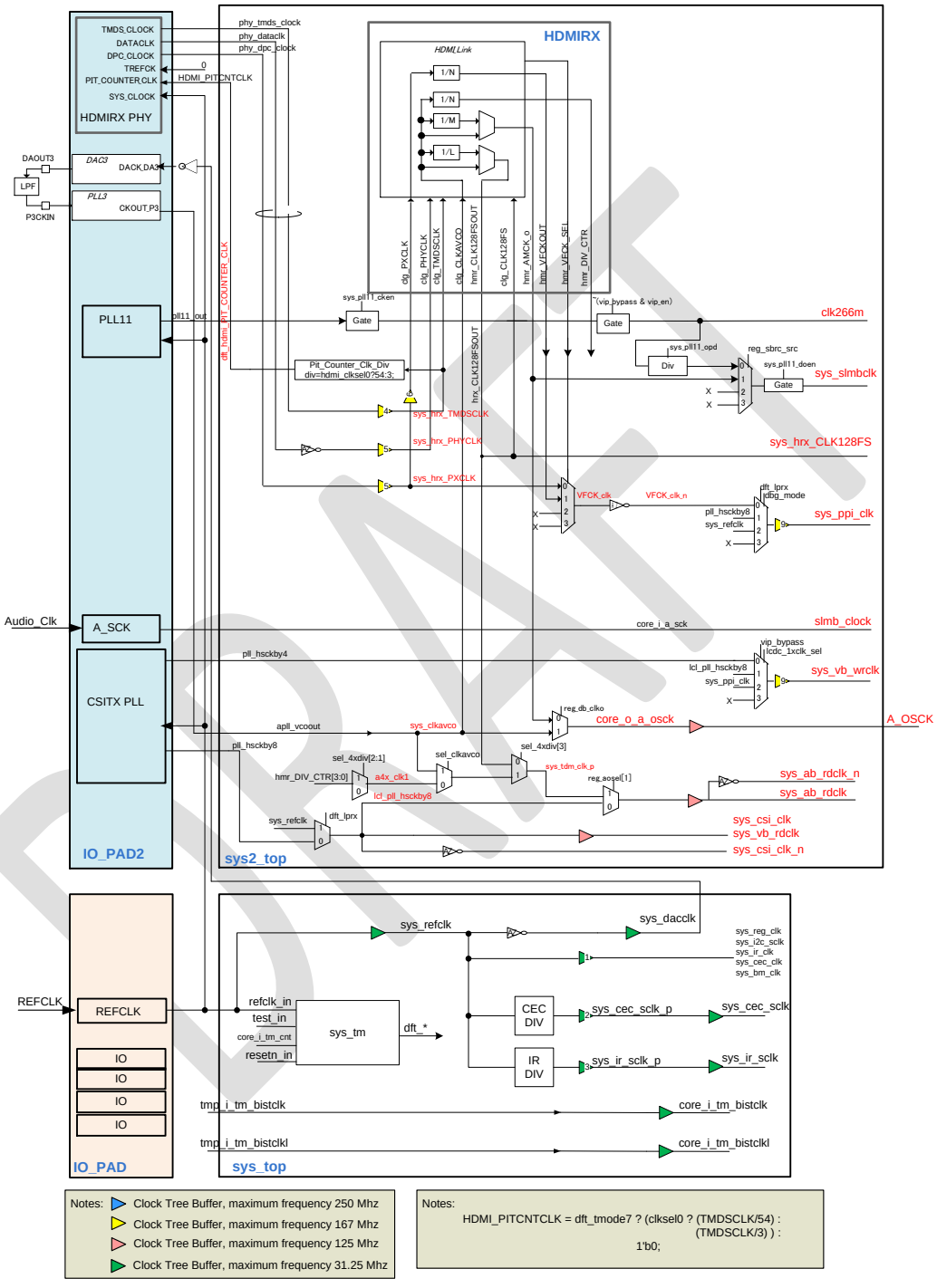


Figure 5-1 Clock Diagram

5.4 TC358749XBG Deep Sleep Mode

TC358749XBG exhibits a power isolation circuit, which is shown in Figure 5-2 below. The yellow color blocks powered by VDDIO1, VDDIO2 and VDDC1 are always on to monitor IO changes. The green color blocks power suppliers, AVDD33, AVDD12, VDD_MIPI and VDDC2, can be turned off when both register bits ConfCtl.PWRISO and SysCtl.SLEEP are asserted.

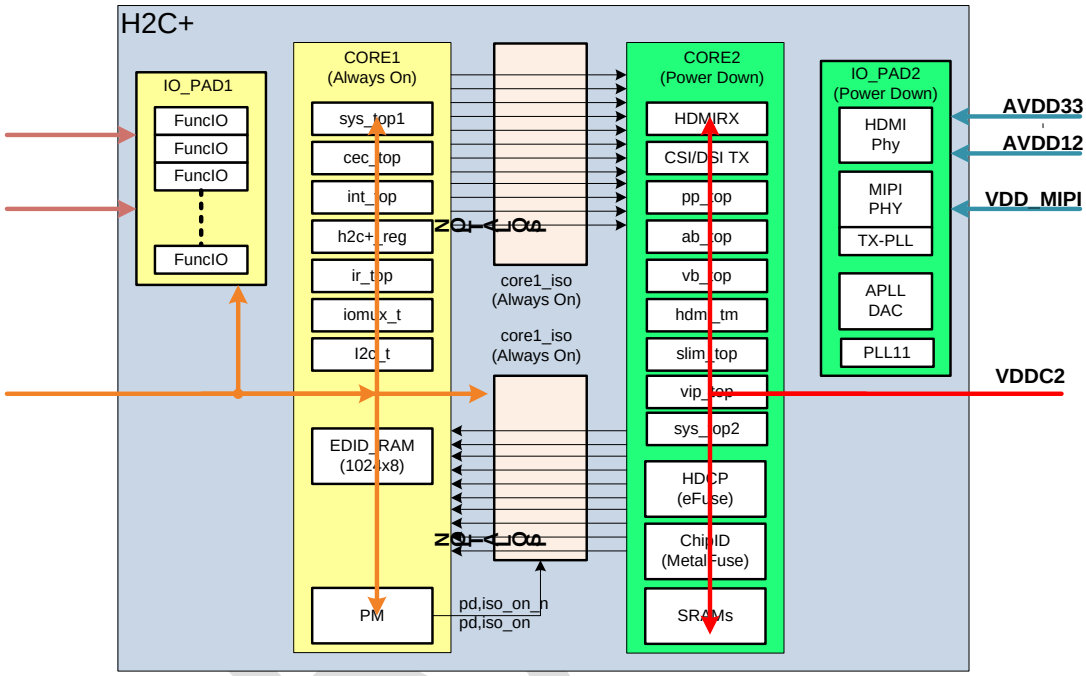


Figure 5-2 Power Isolation Diagram

Enter Deep Sleep State:

1A) Turn on Power Isolation bit (ConfCtl.PWRISO =1)
2A) Make sure there is no activity in TC358749XBG
3A) Turn on Sleep bit (SysCtl.SLEEP = 1)
4A) Shut down the CORE2 power on the board

Exit Deep Sleep State:

1B) Turn on the CORE2 power on the board
2B) Turn off Sleep bit (SysCtl.SLEEP=0)
3B) Wait 1ms for PLL to lock
4B) Re-program all CSI-2TX and HDMIRX registers
5B) Start operation

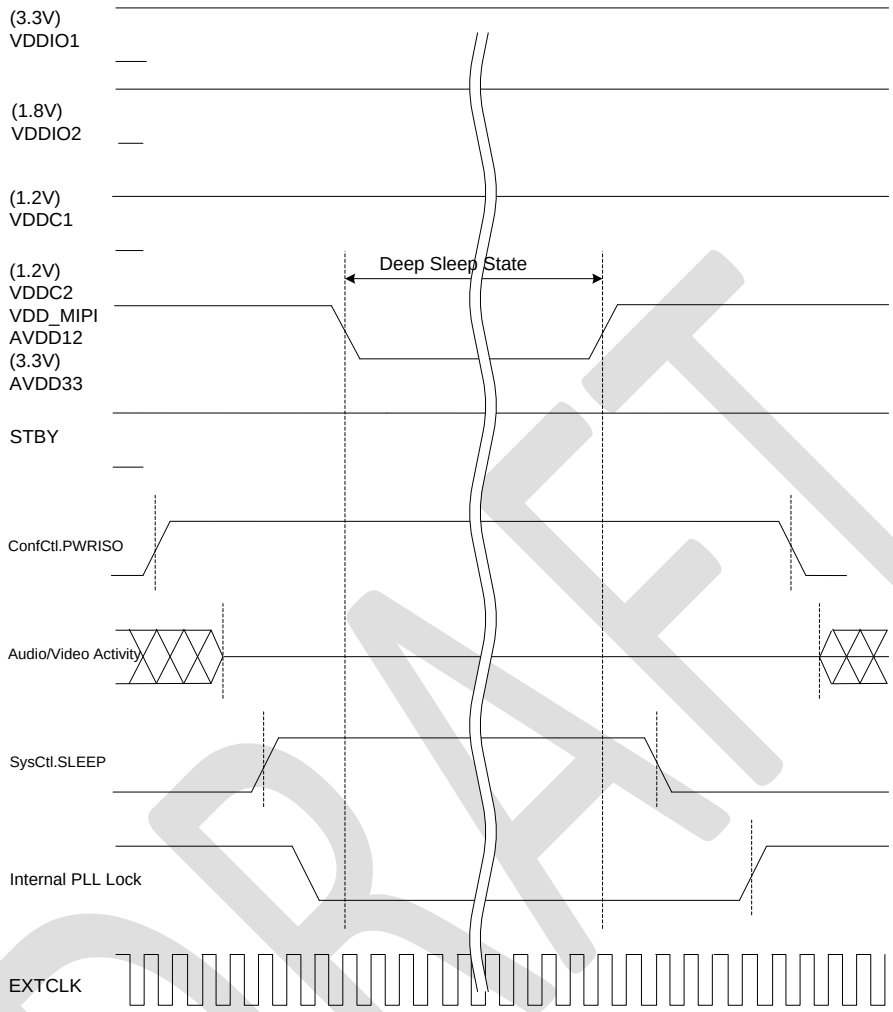


Figure 5-3 Deep Sleep Entry-Exit Sequence

Note: Sleep State is entered by setting (SysCtl.SLEEP = 1 and ConfCtl.PWRISO = 0), during this state TC358749XBG keeps all its registers settings. Deep Sleep Mode is achieved by programming (SysCtl.SLEEP = 1 and ConfCtl.PWRISO = 1), Host is required to re-initiate TC358749XBG after exiting Deep Sleep State.

5.5 TC358749XBG Power Up Procedure

The following sequence should happen before TC358749XBG is able to operate properly:

1. Apply the 1.8V IO power and assert STBY low at same time.
2. While keeping the STBY Low, apply the 3.3V IO power.
3. Then with STBY still Low, apply the 1.2V core power and MIPI PHY power as shown in Figure 5-4 Power On Sequence.
4. Make STBY High and provide clock sources to TC358749XBG.
   - Please keep all the input signals at either “Hi-z” or “logic low” state before powering on TC358749XBG.
5. REFCLK clock source can be either 27/26 MHz or 42 MHz.
6. De-assert the reset.
7. The timing parameters for Figure 5-4 are tabulated in Table 5-3.

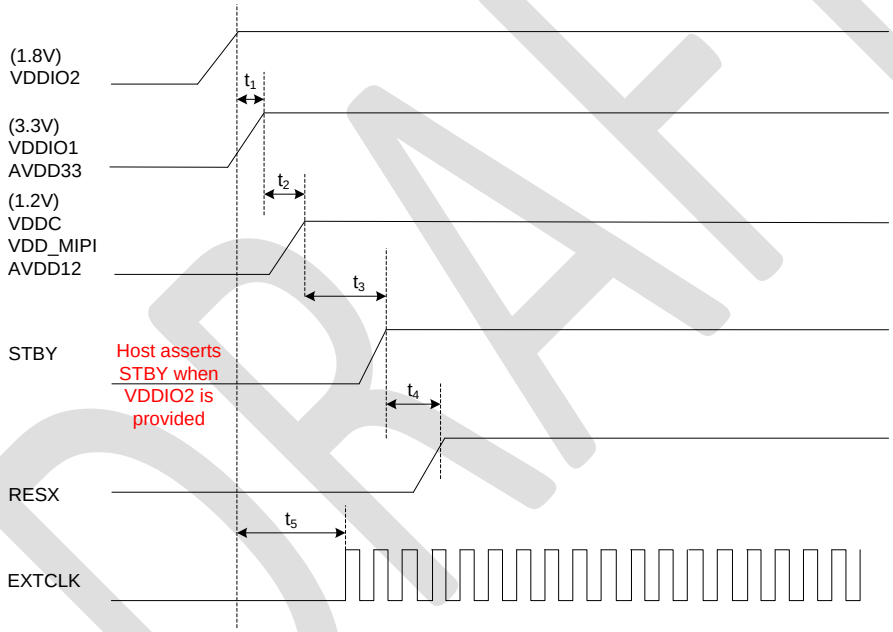


Figure 5-4 Power On Sequence

Table 5-3 Power On Sequence Timing

Parameter	Description	Min.	Typ.	Max.	Units
t1	VDDIO*_33 on delay from VDDIO*_18 on	0	-	-	msec
t2	VDD*_12 on delay from VDDIO*_33 on	0	-	-	msec
t3	STBY “H” delay from VDD*_12 on	0	-	-	msec
t4	RESX release from STBY rise edge	10	-	-	usec
t5	ExtClk Delay from VDDIO*_18 on	0	-	t1+t2+t3	msec

Please keep all the input signals at either “Hi-z” or “logic low” state before powering on VDDIO

5.6 TC358749XBG Power Down Procedure

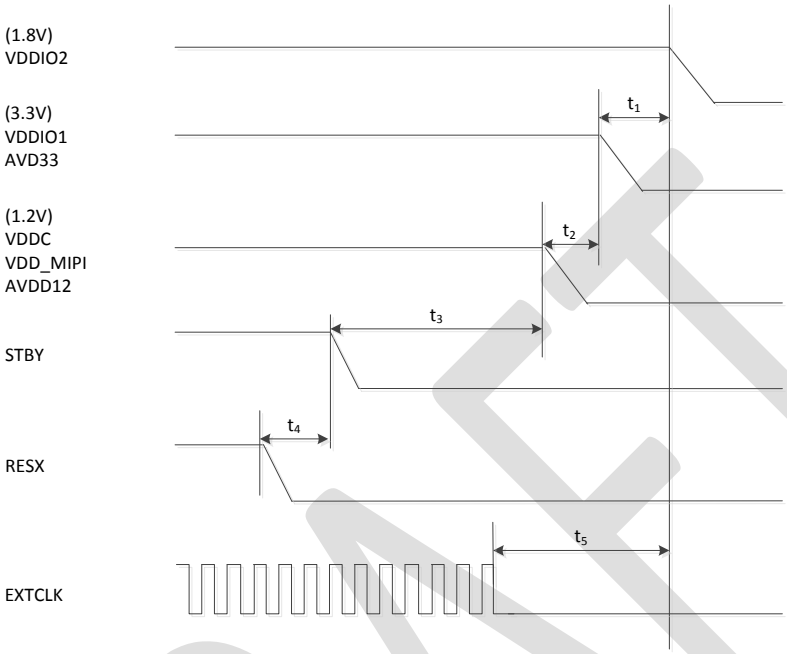


Figure 5-5 Power-Off Sequence Timing

Table 5-4 Power-Off Sequence Timing

Parameter	Description	Min.	Typ.	Max.	Units
t1	VDDIO*_18 off delay from VDDIO*_33 off	0	-	-	msec
t2	VDDIO*_33 off delay from VDDIO*_12 off	0	-	-	msec
t3	VDD*_12 off delay from STBY “L”	0	-	-	msec
t4	RESX assertion delay to STBY “L”	0	-	-	usec
t5	ExtClk Delay delay to VDDIO*_18 off	0	-	t1+t2+t3+t4	msec

Please keep all the input signals at either “Hi-z” or “logic low” state before cutting of VDDIO

6 VIP Programming Modes

6.1 Standard Setting Guide

This section describes the standard settings recommended for the Video IP modules. Flow-chart below shows the decision making for programming different video IP module.

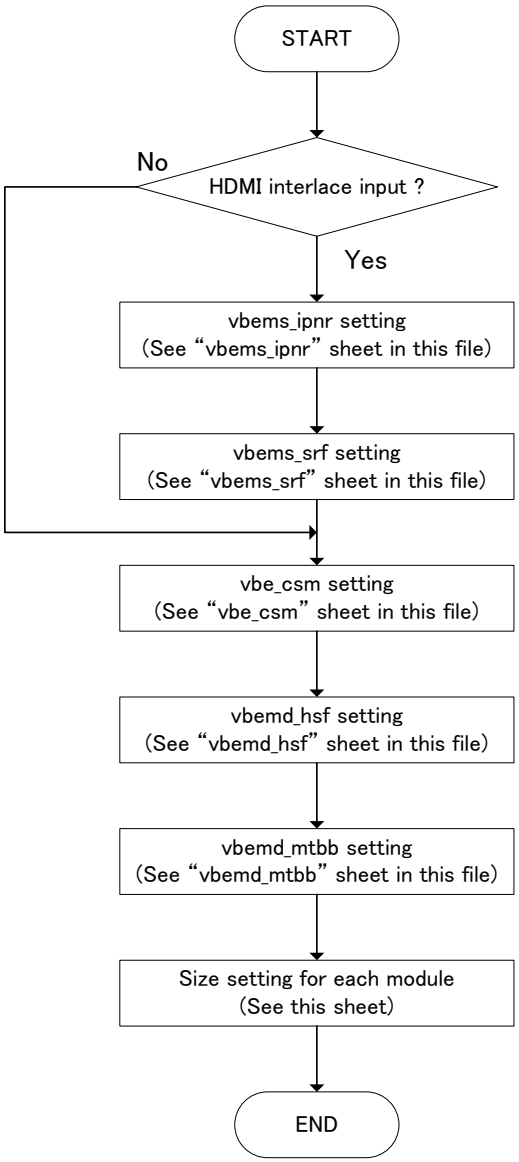


Figure 6-1 Video Modules Programming FlowChart

Below are the recommended filter coefficients for the scalar module for different tap settings.

The recommended tap-settings to be used for scaler are:

1. For horizontal Scaling:
    a. For up-scaling, use 16-tap
    b. For down-scaling, use 8-tap
    c. For no-scaling, use 2-tap (filter co-efficients values ignored).
2. For Vertical Scaling:
    a. For up-scaling, use 8-tap
    b. For down-scaling, use 4-tap
    c. For no-scaling, use 2-tap (filter co-efficients values ignored).

6.2 VIP bypass mode

To bypass the VIP write 1 to VIPCTL: 0x6000, bit position 1 (vip_bypass).

This will completely bypass the VIP module and select the pixel clock for the video buffer input side. TC358749XBG will operate without the video processing, in a similar fashion with TC358743XBG.

6.3 VIP partial bypass mode

Different video blocks of the VIP module can be bypassed independently by setting the appropriate bits in the VBEMS_COM_TEST: 0x4000 control register.

For all of this combination the video buffer will use the CSI-2 clock for the video buffer input side, and the video stream will always go through the vip_fifo and pp_fifo, which will be responsible for the clock domain crossing from the HDMIRX clock to VIP clock and then to CSI-2 clock.

1. When com_ipnr_sel set the interlacer will be bypassed.
2. When com_csf_sel set the scalar will be bypassed.
3. When com_slv_sel set the horizontal scalar will be bypassed.
4. When com_mtx_sel set the color space convertor will be bypassed.

If all video blocks are bypassed, the video stream will go only through the two side FIFO's.

6.4 VIP functional mode

For normal function programming, following sequence is recommended:

1. Wake up, PLL programming, etc. – program PLLCTL1, etc.
2. HDMIRX prog (Optional)
3. RGB to YCbCr conversion (in HDMI Rx)

a. Program registers as mentioned in 4.1.2 Color Space Conversion (RGB to YCbCr)
b. Registers 16'h8573, 16'h8574 & 16'h8576.

4. Program main VIP Control (including 0x6000):
   a. Turn ON/OFF VIP modules
   b. Timing for video blocks start (GO_LINES: 0x6004) i.e. number of (VSW + HPB - 2) lines.
   c. VSYNC delay (VD_DELAY: 0x6008) to account for the pipeline delay through the video blocks, in VIP clock increments.
   d. DE_Size, word count in lines, total pixels in 1 line
   e. FiFo levels for video/audio buffers, etc.
5. Program the LCD Controller parameters.
   a. VSW, VACT, VBP, VFP, HSW, HBP, HACT and HFP
6. VIP modules programming: De-interlacer (If needed)
   a. Refer 7.7.2 De-Interlacer Registers.
7. VIP modules programming: Scaler
   a. Main Scaler registers: Refer 7.7.3 Scaler Registers & 7.7.7 Scaler (additional) Registers.
   b. Additional horizontal Scaler: Refer 7.7.5 Scaler (Horizontal – HSF) Registers
   c. Scaler coefficients: Refer 7.7.8 Scaler Coefficients.
8. VIP modules programming: YCbCr to RGB conversion
   a. Refer 7.7.4 YCbCr to RGB Registers.
9. The last register to be programmed is ConfCtl:0x0004 – VbuffEn, when both HDMIRX and CSI-2 are stable.

6.5 VIP functional mode – 3D Frame-packing

For handling the scaling of 3D Frame-packing format video streams, following additional programming is recommended.

1. Program HDMIRX VS_INS register to insert Vsync into active space.
   a. Set IINS_VS_LINE_SEL_HEN to 1 (HOST setting)
   b. Set INS_VS_HOST_ON to 1 (With Vsync)
   c. Set INS_VS_HEN to 1 (HOST Setting).
2. Set starting line number for dummy Vsync insertion
   a. HDMIRX VS_INS_ST_V0 and VS_INS_ST_V1 registers
3. Set ending line number for Vsync insertion
   a. HDMIRX VS_INS_EN_V0 and VS_INS_EN_V1 registers
4. Enable active space insertion, and set constant pixel value and number of video lines in active space.
   a. VIP VAS register (0x602c)

Note: Two useful status register to monitor are the pp_fifo underflow and vip_fifo overflow, which are part of the VIPCTL: 0x6000 control register. In normal functional mode they should never become 1.

7 RegFile Block (Reg)

The application processor/micro-controller accesses TC358749XBG RegFile block to read status and/or write control registers through the I2C slave interface.

7.1 Register Map

The Overall I2C Offset address map table is provided in below Tables.

Table 7-1 Global Register Map

Segment Address	Module
0x0000 – 0x0013	Global Control Register
0x0014 – 0x001F	Interrupt Register
0x0020 – 0x002B	Clock Control Register
0x002C – 0x00DF	IR Control Register
0x0080 – 0x008F	IO Control Register
0x0100 – 0x01FF	CSI-2-TX PHY Register
0x0200 – 0x03FF	CSI-2-TX PPI Register
0x0400 – 0x05FF	CSI-2-TX Control Register
0x0600 – 0x06FF	CEC Register
0x4000 – 0x6FFF	VIP Register
0x7000 – 0x709F	Internal Color Bar Control Register
0x8500 – 0x851F	HDMIRX Interrupt Control Register
0x8520 – 0x852F	HDMIRX Status Register
0x8530 – 0x85FF	HDMIRX Control Register
0x8600 – 0x86FF	HDMIRX Audio Control Register
0x8700 – 0x87FF	HDMIRX InfoFrame packet data Register
0x8800 – 0x88FF	HDMIRX HDCP Port Register Note: The LSB two bytes indicates the HDCP Offset Registers, e.g. 0x88_15 → HDCP Ainfo Register (x015)
0x8900 – 0x89FF	HDMIRX Video Output Port & 3D Register
0x8B00 – 0x8BFF	YCbCr to RGB Color Space Conversion
0x8C00 – 0x8FFF	HDMIRX EDID-RAM (1024bytes)
0x9000 – 0x90FF	HDMIRX GBD Extraction Control
0x9100 – 0x92FF	HDMIRX GBD RAM read
0xA000 – 0xAFFF	De-Interlacer
0xB000 – 0xBFFF	Scalar

*NOTE: For accessing CSI-2 registers, the **MIPI PLL MUST** be turned on.*

Cells marked yellow are additional registers (to TC358743)

Table 7-2 Detail Register Map

Group	Address	Register	Description
Global (16-bit addressable)	0x0000	ChipID	Chip and Revision ID
	0x0002	SysCtl	System Control Register
	0x0004	ConfCtl	Configuration Control Register
	0x0006	FIFOCtl	FIFO Control Register
	0x000A	VWCnt	Video Word Count Register
	0x001C	AudFrPrem	Audio Frame Preamble Register
	0x001E	SlmbConfig	SLIMbus Configuration Control Register
	0x0020	PLLCtl0	PLL control Register 0
	0x0022	PLLCtl1	PLL control Register 1
	0x0024	PLL11Ctl0	PLL11 control Register 0
	0x0026	PLL11Ctl1	PLL11 control Register 1
	0x0060	CSI-2TX_MISC_CTRL	CSI-2Tx Miscellaneous Control Register
	0x0070	SLMB_AB_THRES	SLIMbus audio threshold Register
	0x0072	I2S_IO_CTL	I2S IO Control Register
	0x0080	IOCtl0	IO control Register 0
	0x0082	IOCtl1	IO control Register 1
	0x0084	I2SPUDCTL	I2S Pull Up/Down Control Register
	0x7082	I2S_CONTROL	I2S Polarity Control
INT (16-bit addressable)	0x0014	IntStatus	Interrupt Status Register
	0x0016	IntMask	Interrupt Mask Register
	0x0018	IntFlag	Interrupt Flag Register
	0x001A	IntSYSStatus	SYS Interrupt status register
IR (16-bit addressable)	0x002C	IrHclk	IR Clock High Time register
	0x002E	IrLclk	IR Clock Low Time register
	0x0034	LCHmin	IR Lead Code Hmin register
	0x0036	LCHmax	IR Lead Code HMax register
	0x0038	LCLmin	IR Lead Code LMin register
	0x003A	LCLmax	IR Lead Code LMax register
	0x003C	BHHmin	IR Bit “H” Hmin register
	0x003E	BHHmax	IR Bit “H” Hmax register
	0x0040	BHLmin	IR Bit “H” Lmin register
	0x0042	BHLmax	IR Bit “H” Lmax register
	0x0044	BLHmin	IR Bit “L” Hmin register
	0x0046	BLHmax	IR Bit “L” Hmax register
	0x0048	BLLmin	IR Bit “L” Lmin register
	0x004A	BLLmax	IR Bit “L” Lmax register
	0x004C	EndHmin	IR “END” Hmin register
	0x004E	EndHmax	IR “END” Hmax register
	0x0050	RCLmin	IR Repeat Code LMin register
	0x0052	RCLmax	IR Repeat Code LMax register
	0x0058	IRCtl	IR Control register
	0x005A	IRRData	IR Receive Data register
	0x7082	IR_CONTROL	IR Input Polarity Control
CSI-2 TX PHY (32-bit addressable)*Note	0x0100	CLW_DPHYCONTTX	Clock Lane DPHY Tx Control register
	0x0104	D0W_DPHYCONTTX	Data Lane0 DPHY Tx Control register
	0x0108	D1W_DPHYCONTTX	Data Lane1 DPHY Tx Control register
	0x010C	D2W_DPHYCONTTX	Data Lane2 DPHY Tx Control register
	0x0110	D3W_DPHYCONTTX	Data Lane3 DPHY Tx Control register

Group	Address	Register	Description
	0x0114 – 0x0123	Reserved	
	0x0124	D0W_DPHYCONTRX	Data Lane0 DPHY Rx Control Register
	0x0126 – 0x0137	Reserved	
	0x0138	COM_DPHYCONTRX	DPHY Rx Common control register
	0x013A – 0x013F	Reserved	
	0x0140	CLW_CNTRL	Clock Lane DPHY Control Register
	0x0144	D0W_CNTRL	Data Lane 0 DPHY Control Register
	0x0148	D1W_CNTRL	Data Lane 1 DPHY Control Register
	0x014C	D2W_CNTRL	Data Lane 2 DPHY Control Register
	0x0150	D3W_CNTRL	Data Lane 3 DPHY Control Register
CSI-2 TX PPI (32-bit addressable)*Note	0x0204	STARTCNTRL	CSI-2 TX Start Control Register
	0x0208	STATUS	CSI-2 TX Status Register
	0x020C	Reserved	
	0x0210	LINEINITCNT	CSI-2 TX Line Initialization Control Register
	0x0214	LPTXTIMECNT	SYSLPTX Timing Generation Counter
	0x0218	TCLK_HEADERCNT	TCLK_ZERO and TCLK_PREPARE Counter
	0x021C	TCLK_TRAILCNT	TCLK_TRAIL Counter
	0x0220	THS_HEADERCNT	THS_ZERO and THS_PREPARE Counter
	0x0224	TWAKEUP	TWAKEUP Counter
	0x0228	TCLK_POSTCNT	TCLK_POST Counter
	0x022C	THS_TRAILCNT	THS_TRAIL Counter
	0x0230	HSTXVREGCNT	TX Voltage Regulator setup Wait Counter
	0x0234	HSTXVREGEN	Voltage regulator enable for HSTX Data Lanes
	0x0238	TXOPTIONCNTRL	TX Option Control
	0x023C	BTACNTRL1	BTA Control
	0x0240 – 0x0243	Reserved	Reserved
	0x0244	D0S_ATMR	D0S_ATMR
	0x0248 – 0x027F	Reserved	Reserved
	0x0280	CLS_PRE	CLS_PRE
	0x0284	D0S_PRE	D0S_PRE
	0x0288	D1S_PRE	D1S_PRE
	0x028C	D2S_PRE	D2S_PRE
	0x0290	D3S_PRE	D3S_PRE
	0x0294 – 0x029F	Reserved	Reserved
	0x02A0	CLS_PREP	CLS_PREP
	0x02A4	D0S_PREP	D0S_PREP
	0x02A8	D1S_PREP	D1S_PREP
	0x02AC	D2S_PREP	D2S_PREP
	0x02B0	D3S_PREP	D3S_PREP
	0x02B4 – 0x02BF	Reserved	Reserved
	0x02C0	CLS_ZERO	CLS_ZERO
	0x02C4	D0S_ZERO	D0S_ZERO
	0x02C8	D1S_ZERO	D1S_ZERO
	0x02CC	D2S_ZERO	D2S_ZERO
	0x02D0	D3S_ZERO	D3S_ZERO
	0x02D4 – 0x02DF	Reserved	Reserved
	0x02E0	PPI_CLRFLG	PPI_CLRFLG
	0x02E4	PPI_CLRSIPO	PPI_CLRSIPO
	0x02E8 – 0x03FF	Reserved	
CSI-2	0x0400-	Reserved	

Group	Address	Register	Description
TX CTRL (32-bit addressable)*Note	0x0408		
	0x040C	CSI-2_CONTROL	CSI-2 Configuration Read Register
	0x0410	CSI-2_STATUS	CSI-2 Status Register
	0x0414	CSI-2_INT	CSI-2TX – Presents interrupts currently being held
	0x0418	CSI-2_INT_ENA	CSI-2TX – Enables CSI-2_INT interrupt source
	0x0430	CSI-2CMD_RDFIFO	CSI-2 Command Read Data FIFO
	0x0434	CSI-2_ACKERR	CSI-2TX – acknowledge error packet
	0x0438	CSI-2_ACKERR_INTENA	CSI-2TX – acknowledge error packet interrupt enable
	0x043C	CSI-2_ACKERR_HALT	CSI-2TX –stop on error bit set in the CSI-2_ACKERR register
	0x0440	CSI-2_RXERR	CSI-2TX – internal error while receiving by the previous BTA
	0x0444	CSI-2_RXERR_INTENA	CSI-2TX –interrupt enable bits of the CSI-2_RXERR register
	0x0448	CSI-2_RXERR_HALT	CSI-2TX – stop on error bit set in the CSI-2_RXERR register
	0x044C	CSI-2_ERR	CSI-2TX – transfer general errors
	0x0450	CSI-2_ERR_INTENA	CSI-2TX – interrupt enable bits of the CSI-2_ERR register
	0x0454	CSI-2_ERR_HALT	CSI-2TX – stop on error bit set in the CSI-2_ERR register
	0x0500	CSI-2_CONFW	CSI-2 TX Configure Write Register
	0x0500 *	CSI-2_LPCMD	CSI-2 LP Command Register (shares address with CSI-2_CONFW)
	0x0504	CSI-2_RESET	CSI-2TX – reset he module and the Receive FIFO content
	0x050C	CSI-2_INT_CLR	CSI-2TX – Clears particular bits of the CSI-2_INT register
	0x0518	CSI-2_START	CSI-2 – Starts CSI-2-TX operation
	0x051A – 0x05FF	Reserved	
CEC (16-bit addressable)	0x0028	CecHclk	CEC Clock High Time register
	0x002A	CecLclk	CEC Clock Low Time register
CEC (32-bit addressable)	0x0600	CECEN	CEC Enable Register
	0x0604	CECADD	CEC Logical Address Register
	0x0608	CECRESET	CEC Reset Register
	0x060C	CECREN	CEC Receive Enable Register
	0x0610	--	Reserved
	0x0614	CECRCR1	CEC Receive Control Register 1
	0x0618	CECRCR2	CEC Receive Control Register 2
	0x061C	CECRCR3	CEC Receive Control Register 3
	0x0620	CECTEN	CEC Transmit Enable Register
	0x0628	CECTCR	CEC Transmit Control Register
	0x062C	CECRSTAT	Receive Interrupt Status Register
	0x0630	CECTSTAT	Transmit Interrupt Status Register
	0x0634	CECRBUF01	CEC Receive Buffer Register 1
	…	…	CEC Receive Buffer Register …
	0x0670	CECRBUF16	CEC Receive Buffer Register 16
	0x0674	CECTBUF01	CEC Transmit Buffer Register 1
	…	…	CEC Transmit Buffer Register …
	0x06B0	CECTBUF16	CEC Transmit Buffer Register 16
	0x06B4	CECRCTR	CEC Receive Byte Counter
	0x06B8	CECTESTR	CEC Test Purpose Register
	0x06C0	CECIMSC	CEC interrupt mask control register
	0x06CC	CECICR	CEC interrupt clear control register
	0x06D0 – 0x06FF	---	Reserved
	0x0702	CSI-2_VSW	CSI-2 Vsync Width register
	0x0704	CSI-2_VBPR	CSI-2 Vsync Back Porch lines register
	0x0706	CSI-2_VACT	CSI-2 Vsync Active lines register
	0x0708	CSI-2_HSW	CSI-2 Hsync Width register
	0x070A	CSI-2_HBPR	CSI-2 Hsync Back Porch register
	0x070C	DCSCMD_TYPE	DCS Command Packet Type register
	0x070E	DCSCMD_WC	DCS Command Packet Word Count
	0x0710	DCSCMD_WD0	DCS Command Packet Data register 0

Group	Address	Register	Description
	0x0712	DCSCMD_WD1	DCS Command Packet Data register 1
	0x0714	DCSCMD_WD2	DCS Command Packet Data register 2
	0x0716	DCSCMD_WD3	DCS Command Packet Data register 3
	…	…	DCS Command Packet Data register …
	0x078A	DCSCMD_WD61	DCS Command Packet Data register 61
	0x078C	DCSCMD_WD62	DCS Command Packet Data register 62
	0x078E	DCSCMD_WD63	DCS Command Packet Data register 63
	0x0790	CSI-2VSSDT	CSI-2 VSync Start Packet Data
	0x0792 – 0x0FFF	Reserved	
	0x1000 – 0x3FFF	Reserved	
VIP Registers (32-bit addressable)	0x4000	VBEMS_COM_TEST	VBEMS_COM_TEST
	0x4080	VBEMS_IP_FIELDID	VBEMS_IP_FIELDID
	0x4084	VBEMS_IP_MAIN_CNT	VBEMS_IP_MAIN_CNT
	0x4088	VBEMS_IP_SRC_WIDTH	VBEMS_IP_SRC_WIDTH
	0x408C	VBEMS_IP_SRC_HEIGHT	VBEMS_IP_SRC_HEIGHT
	0x416C	VBEMS_IP_IP_SIP_MODE	VBEMS_IP_IP_SIP_MODE
	0x4170	VBEMS_IP_IP_SIP_EDGLEV	VBEMS_IP_IP_SIP_EDGLEV
	0x4174	VBEMS_IP_IP_SIP_DLEV	VBEMS_IP_IP_SIP_DLEV
	0x4178	VBEMS_IP_IP_SIP_IKC	VBEMS_IP_IP_SIP_IKC
	0x4180	VBEMS_IP_IP_C_CNT	VBEMS_IP_IP_C_CNT
	0x4204	VBEMS_IP_2322_TEST	VBEMS_IP_2322_TEST
	0x4380	VBEMS_SR_MODE	VBEMS_SR_MODE
	0x4384	VBEMS_SR_HVSZIN	VBEMS_SR_HVSZIN
	0x4484	VBEMS_DE_SIZE	VBEMS_DE_SIZE
	0x4C84	VBEMS_DE_SIZE	VBEMS_DE_SIZE
	0x5040	VBEMS_CS_MODE	VBEMS_CS_MODE
	0x5044	VBEMS_CS_YHVSIN	VBEMS_CS_YHVSIN
	0x5048	VBEMS_CS_CHVSIN	VBEMS_CS_CHVSIN
	0x504C	VBEMS_CS_HSZOUT	VBEMS_CS_HSZOUT
	0x5050	VBEMS_CS_YHFILMODE	VBEMS_CS_YHFILMODE
	0x5054	VBEMS_CS_YHFILPSMODE	VBEMS_CS_YHFILPSMODE
	0x505C	VBEMS_CS_YMHFILBASE	VBEMS_CS_YMHFILBASE
	0x5060	VBEMS_CS_YLHFILBASE	VBEMS_CS_YLHFILBASE
	0x5070	VBEMS_CS_CHFILMODE	VBEMS_CS_CHFILMODE
	0x5074	VBEMS_CS_CHFILPSMODE	VBEMS_CS_CHFILPSMODE
	0x5078	VBEMS_CS_CPHOS	VBEMS_CS_CPHOS
	0x507C	VBEMS_CS_CMHFILBASE	VBEMS_CS_CMHFILBASE
	0x5080	VBEMS_CS_CLHFILBASE	VBEMS_CS_CLHFILBASE
	0x5090	VBEMS_CS_YVFILMODE	VBEMS_CS_YVFILMODE
	0x5094	VBEMS_CS_YVFILPSMODE	VBEMS_CS_YVFILPSMODE
	0x5098	VBEMS_CS_YPVOS_TOP	VBEMS_CS_YPVOS_TOP
	0x509C	VBEMS_CS_YVFILBASE	VBEMS_CS_YVFILBASE
	0x50A0	VBEMS_CS_CVFILMODE	VBEMS_CS_CVFILMODE
	0x50A4	VBEMS_CS_CVFILPSMODE	VBEMS_CS_CVFILPSMODE
	0x50A8	VBEMS_CS_CPVOS_TOP	VBEMS_CS_CPVOS_TOP
	0x50AC	VBEMS_CS_CVFILBASE	VBEMS_CS_CVFILBASE
	0x50B0	VBEMS_CS_YPVOS_BOTTOM	VBEMS_CS_YPVOS_BOTTOM
	0x50B4	VBEMS_CS_CPVOS_BOTTOM	VBEMS_CS_CPVOS_BOTTOM
	0x50B8	VBEMS_CS_PVOS_SELECT	VBEMS_CS_PVOS_SELECT
	0x5204	VBEMS_MTB_ENABLE	VBEMS_MTB_ENABLE
	0x5208	VBEMS_MTB_Y_OFFSET	VBEMS_MTB_Y_OFFSET
	0x520C	VBEMS_MTB_G1	VBEMS_MTB_G1
	0x5210	VBEMS_MTB_G2	VBEMS_MTB_G2
	0x5214	VBEMS_MTB_G_OFFSET	VBEMS_MTB_G_OFFSET
	0x5218	VBEMS_MTB_CB_OFFSET	VBEMS_MTB_CB_OFFSET

Group	Address	Register	Description
	0x521C	VBEMS_MTB_B1	VBEMS_MTB_B1
	0x5220	VBEMS_MTB_B2	VBEMS_MTB_B2
	0x5224	VBEMS_MTB_B_OFFSET	VBEMS_MTB_B_OFFSET
	0x5228	VBEMS_MTB_CR_OFFSET	VBEMS_MTB_CR_OFFSET
	0x522C	VBEMS_MTB_R1	VBEMS_MTB_R1
	0x5230	VBEMS_MTB_R2	VBEMS_MTB_R2
	0x5234	VBEMS_MTB_R_OFFSET	VBEMS_MTB_R_OFFSET
	0x6000	vip_control	VIP Control Register
	0x6004	go_lines	GO Lines Register
	0x6008	vd_delay	VD Delay Register
	0x600C	vip_vsw	vip_vsw
	0x6010	vip_vbp	vip_vbp
	0x6014	vip_val	vip_val
	0x6018	vip_vfp	vip_vfp
	0x601C	vip_hsw	vip_hsw
	0x6020	vip_hbp	vip_hbp
	0x6024	vip_hap	vip_hap
	0x6028	vip_hfp	vip_hfp
	0x602C	vip_vas	vip_vas
	0x6030	cs_vdMYH	cs_vdMYH
	0x6034	cs_vdMYV	cs_vdMYV
	0x6038	cs_vdMCH	cs_vdMCH
	0x603C	cs_vdMCV	cs_vdMCV
	0x6100	YH0_1	YH0_1
	0x6104	YH2_3	YH2_3
	0x6108	YH4_5	YH4_5
	…	…	YH …
	0x61F4	YH122_123	YH122_123
	0x61F8	YH124_125	YH124_125
	0x61FC	YH126_127	YH126_127
	0x6200	YV0_1	YV0_1
	0x6204	YV2_3	YV2_3
	0x6208	YV4_5	YV4_5
	…	…	YV …
	0x62F4	YV122_123	YV122_123
	0x62F8	YV124_125	YV124_125
	0x62FC	YV126_127	YV126_127
	0x6300	CH0_1	CH0_1
	0x6304	CH2_3	CH2_3
	0x6308	CH4_5	CH4_5
	…	…	CH …
	0x63F4	CH122_123	CH122_123
	0x63F8	CH124_125	CH124_125
	0x63FC	CH126_127	CH126_127
	0x6400	CV0_1	CV0_1
	0x6404	CV2_3	CV2_3
	0x6408	CV4_5	CV4_5
	…	…	CV …
	0x64F4	CV122_123	CV122_123
	0x64F8	CV124_125	CV124_125
	0x64FC	CV126_127	CV126_127
	0x6500	VIP_DEBUG	VIP_DEBUG
	0x6504	VIP_FIFO_THRESHOLD	VIP_FIFO_THRESHOLD
	0x6508	PP_FIFO_THRESHOLD	PP_FIFO_THRESHOLD
	0x650C	VIP_INITIAL_DELAY	VIP_INITIAL_DELAY
	0x6510	PP_FIFO_THRESHOLD_REACH	PP_FIFO_THRESHOLD_REACH
	0x6514	VIP_FIFO_MAX_UTIL	VIP_FIFO_MAX_UTIL
	0x6518	VIP_FIFO_MIN_UTIL	VIP_FIFO_MIN_UTIL

Group	Address	Register	Description
	0x651C	PP_FIFO_MAX_UTIL	PP_FIFO_MAX_UTIL
	0x6520	PP_FIFO_MIN_UTIL	PP_FIFO_MIN_UTIL
	0x6524	VIP_FIFO_PIXEL	VIP_FIFO_PIXEL
	0x6528	PP_FIFO_PIXEL	PP_FIFO_PIXEL
	0x6530	VIP_3D_CTRL	VIP_3D_CTRL
	0x6534	TOP_INPUT_PIXEL	TOP_INPUT_PIXEL
	0x6538	TOP_OUTPUT_PIXEL	TOP_OUTPUT_PIXEL
	0x653C	VIP_HAS	VIP_HAS
	0x6540 – 0x6FFF	Reserved	
Internal Colorbar & Debug Registers (8 or 16-bit addressable)	0x7000	DB_Data	Debug Data Register
	0x7004 – 0x707F	Reserved	
	0x7080	DB_Ctl	Debug Control Register
	0x7084	SchkReg1	Self-Check 1 Register
	0x7086	SchkReg2	Self-Check 2 Register
	0x7090	DAVLCreg	Debug Active Line Count Register
	0x7092	DAWCreg	Debug Line Width Register
	0x7094	DVBCreg	Debug Vertical Blank Line Count Register
	0x7096 – 0x84FF	Reserved	
HDMI RX Interrupts (8-bit addressable)	0x8500	HDMI_INT0	HDMI Interrupt 0
	0x8501	HDMI_INT1	HDMI Interrupt 1
	0x8502	SYS_INT	System Interrupt
	0x8503	CLK_INT	Clock Interrupt
	0x8504	PACKET_INT	Packet Interrupt
	0x8505	CBIT_INT	CBIT Interrupt
	0x8506	AUDIO_INT	AUDIO Interrupt
	0x8507	ERR_INT	ERROR Interrupt
	0x8508	HDCP_INT	HDCP Interrupt
	0x8509	GBD_INT	GBD Interrupt
	0x850a	PHYERR_INT	PHY ERROR Interrupt
	0x850b	MISC_INT	MISCELLANEOUS Interrupt
	0x850f	KEY_INT	KEY Interrupt
	0x8512	SYS_INTM	SYSTEM Interrupt Mask
	0x8513	CLK_INTM	CLOCK Interrupt Mask
	0x8514	PACKET_INTM	PACKET Interrupt Mask
	0x8515	CBIT_INTM	CBit Interrupt Mask
	0x8516	AUDIO_INTM	Audio Interrupt Mask
	0x8517	ERR_INTM	ERROR Interrupt Mask
	0x8518	HDCP_INTM	HDCP Interrupt Mask
	0x8519	GBD_INTM	GBD Interrupt Mask
	0x851b	MISC_INTM	MISCELLANEOUS Interrupt Mask
	0x851f	KEY_INTM	KEY Interrupt Mask
HDMI RX Status (8-bit addressable)	0x8520	SYS_STATUS	SYS Status
	0x8521	VI_STATUS0	Input Video Signal Status 0
	0x8522	VI_STATUS1	Input Video Signal Status 1
	0x8523	AU_STATUS0	AUDIO Status 0
	0x8524	AU_STATUS1	AUDIO Status 1
	0x8525	VI_STATUS2	Input Video Signal Status 2
	0x8526	CLK_STATUS	CLOCK Status
	0x8527	PHYERR_STATUS	PHY ERROR Status
	0x8528	VI_STATUS3	Input Video Signal Status 3
HDMI	0x8531	PHY_CTL0	PHY Control 0

Group	Address	Register	Description
RX Control (8-bit addressable)	0x8534	PHY_EN	PHY Enable
	0x8535	PHY_RST	PHY Reset
	0x8538	PHY_PLL	PHY PLL
	0x853a	PHY_CDR	PHY CDR
	0x8540	SYS_FREQ0	SYS FREQ0 Register
	0x8541	SYS_FREQ1	SYS FREQ1 Register
	0x8543	DDC_CTL	DDC Control
	0x8544	HPD_CTL	HPD Control
	0x8545	ANA_CTL	ANA Control
	0x8546	AVM_CTL	AVMUTE Control
	0x8547	SOFT_RST	Software Reset
	0x854A	INIT_END	INIT END
	0x8560	HDCP_MODE	HDCP Operation Mode
	0x8561	HDCP_CMD	HDCP Command
	0x8570	VI_MODE	VI MODE Register
	0x8573	VOUT_SET	VOUT_SET Register
	0x8574	VOUT_SET3	VOUT_SET3 Register
	0x8576	VOUT_COLOR_SEL	VOUT_COLOR_SEL Register
	0x8577	DC_MODE	DC MODE Register
HDMI RX Audio Control (8-bit addressable)	0x8600	FORCE_MUTE	FORCE MUTE
	0x8601	CMD_AUD	CMD AUD
	0x8602	AUTO_CMD0	Audio Auto Mute
	0x8603	AUTO_CMD1	Audio Auto Mute
	0x8604	AUTO_CMD2	Audio Auto Play
	0x8606	BUFINIT_START	Audio Buffer Init Start time
	0x8607	FS_MUTE	Audio Sample MUTE
	0x8620	FS_IMODE	Audio Sample Frequency Input Mode
	0x8621	FS_SET	Audio Sample Frequency Mode
	0x8630	LOCKDET_REF0	RefClk Cycle numbers [7:0] for 10 ms
	0x8631	LOCKDET_REF1	RefClk Cycle numbers [15:8] for 10 ms
	0x8632	LOCKDET_REF2	RefClk Cycle numbers [19:16] for 10 ms
	0x8640	ACR_MODE	CTS Adjustment Mode
	0x8641	ACR_MDF0	CTS Adjustment Amount0
	0x8642	ACR_MDF1	CTS Adjustment Amount1
	0x8651	SDO_MODE0	SDO_MODE0
	0x8652	SDO_MODE1	SDO_MODE1
	0x8656	SDO_CHSEL3	SDO_CHSEL3
	0x8665	DIV_MODE	DIV_MODE Register
	0x8666	DIV_CLK	DIV_CLK Register
	0x8667	DIV24_SEL	DIV24_SEL Register
	0x8668	DIV32_SEL	DIV32_SEL Register
	0x8669	DIV48_SEL	DIV48_SEL Register
	0x866A	DIV96_SEL	DIV96_SEL Register
	0x866B	DIV192_SEL	DIV192_SEL Register
	0x866C	DIV768_SEL	DIV768_SEL Register
	0x866D	DIV384_SEL	DIV384_SEL Register
	0x8670	NCO_F0_MOD	Audio PLL Setting Register
	0x8671	NCO_48F0A	Audio PLL Setting Register
	0x8672	NCO_48F0B	Audio PLL Setting Register
	0x8673	NCO_48F0C	Audio PLL Setting Register
	0x8674	NCO_48F0D	Audio PLL Setting Register
	0x8675	NCO_44F0A	Audio PLL Setting Register
	0x8676	NCO_44F0B	Audio PLL Setting Register
	0x8677	NCO_44F0C	Audio PLL Setting Register
	0x8678	NCO_44F0D	Audio PLL Setting Register
	0x8680	EX_MODE	EX_MODE Register
	0x8690	APIN_EN0	Audio Output Module Terminal Control

Group	Address	Register	Description
HDMI RX Info Frame Data (8-bit addressable)	0x8701	TYP_VS_SET	VS_info Packet Type code setting
	0x8702	TYP_AVI_SET	AVI_info Packet Type code setting
	0x8703	TYP_SPD_SET	SPD_info Packet Type code setting
	0x8704	TYP_AUD_SET	AUD_info Packet Type code setting
	0x8705	TYP_MS_SET	MS_info Packet Type code setting
	0x8706	TYP_ACP_SET	ACP Packet Type code setting
	0x8707	TYP_ISRC1_SET	ISRC1 Packet Type code setting
	0x8708	TYP_ISRC2_SET	ISRC2 Packet Type code setting
	0x8709	PK_INT_MODE	Packet Interrupt Mode
	0x870a	PK_AUTO_CLR	Packet Auto Clear
	0x870b	NO_PK_LIMIT	No Packet Limit
	0x870c	NO_PK_CLR	No Packet Clear
	0x870d	ERR_PK_LIMIT	Error Packet Limit
	0x870e	NO_PK_LIMIT2	No Packet Limit 2
	0x870f	VS_IEEE_SEL	VS IEEE Select
	0x8710	PK_AVI_0HEAD	861B AVI_info packet Header byte 0
	0x8711	PK_AVI_1HEAD	861B AVI_info packet Header byte 1
	0x8712	PK_AVI_2HEAD	861B AVI_info packet Header byte 2
	0x8713	PK_AVI_0BYTE	861B AVI_info packet Data byte 0
	0x8714	PK_AVI_1BYTE	861B AVI_info packet Data byte 1
	0x8715	PK_AVI_2BYTE	861B AVI_info packet Data byte 2
	…	…	861B AVI_info packet Data byte …
	0x8721	PK_AVI_14BYTE	861B AVI_info packet Data byte 14
	0x8722	PK_AVI_15BYTE	861B AVI_info packet Data byte 15
	0x8723	PK_AVI_16BYTE	861B AVI_info packet Data byte 16
	0x8730	PK_AUD_0HEAD	861B AUD_info packet Header byte 0
	0x8731	PK_AUD_1HEAD	861B AUD_info packet Header byte 1
	0x8732	PK_AUD_2HEAD	861B AUD_info packet Header byte 2
	0x8733	PK_AUD_0BYTE	861B AUD_info packet Data byte 0
	0x8734	PK_AUD_1BYTE	861B AUD_info packet Data byte 1
	0x8735	PK_AUD_2BYTE	861B AUD_info packet Data byte 2
	…	…	861B AUD_info packet Data byte …
	0x873b	PK_AUD_8BYTE	861B AUD_info packet Data byte 8
	0x873c	PK_AUD_9BYTE	861B AUD_info packet Data byte 9
	0x873d	PK_AUD_10BYTE	861B AUD_info packet Data byte 10
	0x8740	PK_MS_0HEAD	861B MS_info packet Header byte 0
	0x8741	PK_MS_1HEAD	861B MS_info packet Header byte 1
	0x8742	PK_MS_2HEAD	861B MS_info packet Header byte 2
	0x8743	PK_MS_0BYTE	861B MS_info packet Data byte 0
	0x8744	PK_MS_1BYTE	861B MS_info packet Data byte 1
	0x8745	PK_MS_2BYTE	861B MS_info packet Data byte 2
	…	…	861B MS_info packet Data byte …
	0x874b	PK_MS_8BYTE	861B MS_info packet Data byte 8
	0x874c	PK_MS_9BYTE	861B MS_info packet Data byte 9
	0x874d	PK_MS_10BYTE	861B MS_info packet Data byte 10
	0x8750	PK_SPD_0HEAD	861B SPD_info packet Header byte 0
	0x8751	PK_SPD_1HEAD	861B SPD_info packet Header byte 1
	0x8752	PK_SPD_2HEAD	861B SPD_info packet Header byte 2
	0x8753	PK_SPD_0BYTE	861B SPD_info packet Data byte 0
	0x8754	PK_SPD_1BYTE	861B SPD_info packet Data byte 1
	0x8755	PK_SPD_2BYTE	861B SPD_info packet Data byte 2
	…	…	861B SPD_info packet Data byte …
	0x876c	PK_SPD_25BYTE	861B SPD_info packet Data byte 25
	0x876d	PK_SPD_26BYTE	861B SPD_info packet Data byte 26
	0x876e	PK_SPD_27BYTE	861B SPD_info packet Data byte 27
	0x8770	PK_VS_0HEAD	861B VS_info packet Header byte 0
	0x8771	PK_VS_1HEAD	861B VS_info packet Header byte 1

Group	Address	Register	Description
	0x8772	PK_VS_2HEAD	861B VS_info packet Header byte 2
	0x8773	PK_VS_0BYTE	861B VS_info packet Data byte 0
	0x8774	PK_VS_1BYTE	861B VS_info packet Data byte 1
	0x8775	PK_VS_2BYTE	861B VS_info packet Data byte 2
	…	…	861B VS_info packet Data byte …
	0x878c	PK_VS_25BYTE	861B VS_info packet Data byte 25
	0x878d	PK_VS_26BYTE	861B VS_info packet Data byte 26
	0x878e	PK_VS_27BYTE	861B VS_info packet Data byte 27
	0x8790	PK_ACP_0HEAD	861B ACP_info packet Header byte 0
	0x8791	PK_ACP_1HEAD	861B ACP_info packet Header byte 1
	0x8792	PK_ACP_2HEAD	861B ACP_info packet Header byte 2
	0x8793	PK_ACP_0BYTE	861B ACP_info packet Data byte 0
	0x8794	PK_ACP_1BYTE	861B ACP_info packet Data byte 1
	0x8795	PK_ACP_2BYTE	861B ACP_info packet Data byte 2
	…	…	861B ACP_info packet Data byte …
	0x87ac	PK_ACP_25BYTE	861B ACP_info packet Data byte 25
	0x87ad	PK_ACP_26BYTE	861B ACP_info packet Data byte 26
	0x87ae	PK_ACP_27BYTE	861B ACP_info packet Data byte 27
	0x87b0	PK_ISRC1_0HEAD	861B ISRC1_info packet Header byte 0
	0x87b1	PK_ISRC1_1HEAD	861B ISRC1_info packet Header byte 1
	0x87b2	PK_ISRC1_2HEAD	861B ISRC1_info packet Header byte 2
	0x87b3	PK_ISRC1_0BYTE	861B ISRC1_info packet Data byte 0
	0x87b4	PK_ISRC1_1BYTE	861B ISRC1_info packet Data byte 1
	0x87b5	PK_ISRC1_2BYTE	861B ISRC1_info packet Data byte 2
	…	…	861B ISRC1_info packet Data byte …
	0x87c0	PK_ISRC1_13BYTE	861B ISRC1_info packet Data byte 13
	0x87c1	PK_ISRC1_14BYTE	861B ISRC1_info packet Data byte 14
	0x87c2	PK_ISRC1_15BYTE	861B ISRC1_info packet Data byte 15
	0x87d0	PK_ISRC2_0HEAD	861B ISRC2_info packet Header byte 0
	0x87d1	PK_ISRC2_1HEAD	861B ISRC2_info packet Header byte 1
	0x87d2	PK_ISRC2_2HEAD	861B ISRC2_info packet Header byte 2
	0x87d3	PK_ISRC2_0BYTE	861B ISRC2_info packet Data byte 0
	0x87d4	PK_ISRC2_1BYTE	861B ISRC2_info packet Data byte 1
	0x87d5	PK_ISRC2_2BYTE	861B ISRC2_info packet Data byte 2
	…	…	861B ISRC2_info packet Data byte …
	0x87ec	PK_ISRC2_25BYTE	861B ISRC2_info packet Data byte 25
	0x87ed	PK_ISRC2_26BYTE	861B ISRC2_info packet Data byte 26
	0x87ee	PK_ISRC2_27BYTE	861B ISRC2_info packet Data byte 27
HDCP RX HDCP (8-bit addressable)	0x8800 – 0x8839	XXXX	HDCP Rx Registers at offset 0x00 to 0x39
	0x8840	BCaps	HDCP Rx BCap Registers
	0x8841	BStatus0	HDCP Rx BStatu0
	0x8842	BStatus1	HDCP Rx BStatu0
	0x8843	KSVFIFO	HDCP Rx KSVFIFO Register
	0x8844 - 0x88FF	XXXX	HDCP Rx Registers at offset 0x44 to 0xFF

Note:

- HDMI registers are 8-bit register.
- CEC registers are 32-bit register. Host must write two consecutive 16-bit register write to form 32-bit access.
- Note: CSI-2 registers cannot be accessed when video transfer is in progress.

The following sections provide a detailed description of the registers.

7.2 Global

7.2.1 Chip and Revision ID (ChipID: 0x0000)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ChipID							
Type	RO							
Default	0x47							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	RevID							
Type	RO							
Default	0x0							

Register Field	Bit	Description
ChipID	[15:8]	**Chip ID** Chip ID assigned for this device by Toshiba.
RevID	[7:0]	**Revision ID** Revision ID for this device assigned by Toshiba.

7.2.2 System Control Register (SysCtl: 0x0002)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	ABRst	SLMBRst	VIPRst	IRRst	CecRst	CTxRst	HdmiRst
Type	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I2S_Dis	Reserved						SLEEP
Type	R/W	RO						R/W
Default	0x1	0x0						0x1

Register Field	Bit	Description
Reserved	[15]	
ABRst	[14]	**Audio Block Software Reset (Active high)** This bit is set to force Audio Block logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear ABRst when set.
SLMBRst	[13]	**SLIMbus Software Reset (Active high)** This bit is set to force SLIMbus logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear SLMBRst when set.
VIPRst	[12]	**VIP Software Reset (Active high)** This bit is set to force VIP logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation

Register Field	Bit	Description
		Software needs to clear VIPRst when set.
IRRst	[11]	**IR Software Reset (Active high)** This bit is set to force IR logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear IRReset when set.
CecRst	[10]	**CEC Software Reset (Active high)** This bit is set to force CEC logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear CECReset when set.
CTxRst	9	**CSI-2-TX Software Reset (Active high)** This bit is set to force CSI-2-TX logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear CReset when set.
HdmiRst	8	**HDMI-RX Software Reset (Active high)** This bit is set to force HDMI-RX logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear HReset when set.
I2S_Dis	7	**I2S Interface Disable (Active high)** Control to disable I2S output interface (applies when ConfCtl.SLMB_en=0) 0: Enable I2S output interface 1: Disable I2S output interface Software needs to enable this (disabled by default).
Reserved	[6:1]	
SLEEP	0	**SLEEP** control 0: Normal operation 1: Sleep mode

7.2.3 Configuration Control Register (ConfCtl: 0x0004)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PWRISO	SLMB_en	Reserved	AClkOpt	AudChNum		AudChSel	I2SDlyOpt
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0		0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	YCbCrFmt		Reserved	AudOutSel		AutoIndex	ABufEn	VBufEn
Type	R/W		R/W	R/W		R/W	R/W	R/W
Default	0x0		0x0	0x0		0x0	0x0	0x0

Register Field	Bit	Description
PWRISO	[15]	**Power Island Enable** 1'b0: Normal 1'b1: Power Island Enable To be work with SysCtl.SLEEP, please refer to section 5.4
SLMB_en	[14]	**SLIMbus Enable** 1'b0: Disable SLIMbus output 1'b1: Enable SLIMbus output
Reserved	[13]	Reserved
AClkOpt	[12]	**Audio Bit Clock Option** 1'b0: I2S/TDM clock are free running 1'b1: I2S/TDM clock stops when Mute active
AudChNum	[11:10]	**Audio Channel Output Channels** 2'b00: Enable 8 Audio channels 2'b01: Enable 6 Audio channels 2'b10: Enable 4 Audio channels 2'b11: Enable 2 Audio channels Note: valid only AudChSel = 1
AudChSel	[9]	**Audio Channel Number Selection Mode** 1'b0: Auto detect by HW 1'b1: Select by AudChNum register bits Note: valid only when AudOutSel[4] = 0
I2SDlyOpt	[8]	**I2S/TDM Data Delay Option** 1'b0: No delay 1'b1: Delay by 1 clock
YCbCrFmt	[7:6]	**YCbCr Video Output Format select** 2'b00: Select YCbCr444 data format 2'b01: Select YCbCr422 12-bit data format 2'b10: Internal Generated output pattern, e.g. ColorBar 2'b11: Select YCbCr422 8-bit (HDMI YCbCr422 12-bit data format, discard last 4 data bits) Note: RGB data, this field has to be set to 2'b00
Reserved	[5]	Reserved
AudOutSel	[4:3]	**Audio Output option** 2'b00: Reserved 2'b01: Reserved 2'b10: Audio output to I2S i/f 2'b11: Audio output to TDM i/f
AutoIndex	[2]	**I2C slave index increment** 1'b0: I2C address index does not increment on every data byte transfer 1'b1: I2C address index increments on every data byte transfer
ABufEn	[1]	**Audio TX Buffer Enable** 1'b0: disable 1'b1: enable Note: enable only after HDMIRX and CSI-2TX register have been setup.
VBufEn	[0]	**Video TX Buffer Enable** 1'b0: disable 1'b1: enable Note: enable only after HDMIRX and CSI-2TX register have been setup.

7.2.4 FIFO Control Register (FIFOCtl: 0x0006)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						FIFOLevel[9:8]	
Type	RO						R/W	
Default	0x0						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	FIFOLevel[7:0]							
Type	R/W							
Default	0x10							

Register Field	Bit	Description
Reserved	[15:10]	Reserved
FIFOLevel	[9:0]	**FIFOLevel** This field determines video delay from FiFo level, when reaches to this level FiFo controller asserts FiFoRdy for CSI-2-TX controller to start output

7.2.5 Video Data Word Count Register (VWCnt: 0x000A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	VWordCnt[15:8]							
Type	R/W							
Default	0x01							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VWordCnt[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
VWordCnt	[15:0]	**Video Data Word Count** Defined total number of byte for each line.

7.2.6 Packet ID Register 1 (PacketID1: 0x000C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	VPID1							
Type	R/W							
Default	0x34							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VPID0							
Type	R/W							
Default	0x35							

Register Field	Bit	Description
VPID1	[15:8]	CSI-2 Video Packet ID 1 Note: For interlace mode only, this ID is for Bottom video field.
VPID0	[7:0]	CSI-2 Video Packet ID 0 Note: For interlace mode only, this ID is for Top video field

7.2.7 Packet ID Register 2 (PacketID2: 0x000E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	IFPID							
Type	R/W							
Default	0x36							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							
Type	R/W							
Default	0x37							

Register Field	Bit	Description
IFPID	[15:8]	CSI-2 InfoFrame Packet ID
Reserved	[7:0]	Reserved

7.2.8 Packet ID Register 3 (PacketID3: 0x0010)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VPID2							
Type	R/W							
Default	0x24							

Register Field	Bit	Description
Reserved	[15:8]	
VPID2	[7:0]	CSI-2 Video Packet ID Note: Use when YCbCrFmt[1:0] = 2'b01 or YCbCrFmt[1:0] = 2'b10

7.2.9 Frame Count Control Register (FCCtl: 0x0012)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	FrCnt							
Type	R/W							

Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	FrCnt							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
FrCnt	[15:0]	Frame Count Control Register 16'h0000: Disable Frame Count 16'h0001: Count 1,1,1,1,1, 16'h0002: Count 1,2,1,2,1,2,1,2…. 16'h0003: Count 1,2,3,1,2,3,….. 16'h0004: Count 1,2,3,4,1,2,3,4,1,2,3,4 …. Note: Increment on every HDMI Vsync. "Frame Start" and "Frame End" packet have the same FrameCount number.

7.2.10 Interrupt Status Register (IntStatus: 0x0014)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					AMUTE_INT	HDMI_INT	CSI-2_INT
Type	RO					W1C	W1C	W1C
Default	0x0					0x0	0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	SLMB_INT	Reserved	SYS_INT	CEC_EINT	CEC_TINT	CEC_RINT	IR_EINT	IR_DINT
Type	R/W1C	RO	W1C	W1C	W1C	W1C	W1C	W1C
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:11]	
AMUTE_INT	[10]	Audio Mute Interrupt Status 1'b0: Normal 1'b1: Audio change from Normal to Mute Default = 0 (Value immediately becomes '1' after reset)
HDMI_INT	[9]	HDMI-RX Interrupt Status Note: all HDMI interrupt flags defined in HDMI register space
CSI-2_INT	[8]	CSI-2-TX Interrupt Status
SLMB_INT	[7]	SLIMbus General Interrupt Status
Reserved	[6]	
SYS_INT	[5]	TC358749XBG System Interrupt Status 1'b0: Normal 1'b1: Video/Audio Overflow/Underflow/WakeUp occurs
CEC_EINT	[4]	CEC Error Interrupt Status 1'b0: Normal 1'b1: CEC Errors occurs
CEC_TINT	[3]	CEC Transmit Interrupt Status 1'b0: Idle 1'b1: Transmit completed/done

CEC_RINT	[2]	CEC Receive Interrupt Status 1'b0: Idle 1'b1: Data Received
IR_EINT	[1]	IR Error Interrupt Status 1'b0: No Error 1'b1: Error occurs (overflow error)
IR_DINT	[0]	IR Data Interrupt Status 1'b0: Idle 1'b1: Interrupt occurs (IR Data available)

Note: Write "1" to clear Interrupt. Interrupt is only active when INT_MASK = 1'b0.

Note: Pls. clear the interrupt source first (e.g. CEC interrupt bit in CEC interrupt clear register) before clearing the status bit in this register.

7.2.11 Interrupt Mask Register (IntMask: 0x0016)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					AMUTE_MSK	HDMI_MSK	CSI-2_MSK
Type	RO					R/W	R/W	R/W
Default	0x0					0x1	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SLMB_MSK	Reserved	SYS_MSK	CEC_EMSK	CEC_TMSK	CEC_RMSK	IR_EMSK	IR_DMSK
Type	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:11]	
AMUTE_MSK	[10]	Audio Mute Interrupt Mask
HDMI_MSK	[9]	HDMI-RX Interrupt Mask
CSI-2_MSK	[8]	CSI-2-TX Interrupt Mask
SLMB_MSK	[7]	SLIMbus General Interrupt Mask
Reserved	[6]	
SYS_MSK	[5]	SYS Interrupt Mask
CEC_EMSK	[4]	CEC Error Interrupt Mask
CEC_TMSK	[3]	CEC Transmit Interrupt Mask
CEC_RMSK	[2]	CEC Receive Interrupt Mask
IR_EMSK	[1]	IR Error Interrupt Mask
IR_DMSK	[0]	IR Data Interrupt Mask 1'b0: Enable Interrupt 1'b1: Mask Interrupt

Note: if *MSK=1'b1 then *INT is never asserted

7.2.12 Interrupt Flag Register (IntFlag: 0x0018)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					AMUTE_FLG	HDMI_FLG	CSI-2_FLG
Type	RO					RO	RO	RO
Default	0x0					0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SLMB_FLG	Reserved	SYS_FLG	CEC_EFLG	CEC_TFLG	CEC_RFLG	IR_EFLG	IR_DFLG

Type	RO_S	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:11]	
AMUTE_FLG	[10]	Audio Mute Interrupt Flag Default = 0 (Value immediately becomes '1' after reset)
HDMI_FLG	[9]	HDMI-RX Interrupt Flag
CSI-2_LG	[8]	CSI-2-TX Interrupt Flag
SLMB_FLG	[7]	SLIMbus General Interrupt Flag
Reserved	[6]	
SYS_FLG	[5]	SYS Interrupt Flag
CEC_EFLG	[4]	CEC Error Interrupt Flag
CEC_TFLG	[3]	CEC Transmit Interrupt Flag
CEC_RFLG	[2]	CEC Receive Interrupt Flag
IR_EFLG	[1]	IR Error Interrupt Flag
IR_DFLG	[0]	IR Data Interrupt Flag 1'b0: Idle 1'b1: Interrupt occurs (Data available)

Note: *MASK does not affect these flag status

7.2.13 SYS Interrupt Status Register (IntSYSStatus: 0x001A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HPI_chg	DDC_act	Reserved	Vb_ufl	Vb_ofl
Type	RO			RO	RO	RO	RO	RO
Default	0x0			0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:5]	
HPI_chg	[4]	HPDI status 0: Normal 1: change Note: only valid during sleep mode with Power Island Enable(Deep Sleep mode), use to wake up the host when HDPI is changing.
DDC_act	[3]	DDC interface status 0: idle 1: DDC active Note: (1) only valid during sleep mode with Power Island Enable (Deep Sleep mode), use to wake up the host when DDC interface is active. (2) Host should clear this status only if it finished re-program all the TC358749XBG HDMI/CSI-2TX registers.
Reserved	[2]	
Vb_ufl	[1]	Video Buffer Underflow status 0: Normal 1: Underflow
Vb_ofl	[0]	Video Buffer Overflow status 0: Normal

		1: Overflow

Note: These status will be clear when write “1” to SYS_INT register bit in IntStatus register.

7.2.14 Audio Frame Preamble Register (AudFrPrem: 0x001C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				prem_m			
Type	RO				R/W			
Default	0x0				0x1			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	prem_w				prem_b			
Type	R/W				R/W			
Default	0x2				0x0			

Register Field	Bit	Description
Reserved	[15:12]	
prem_m	[11:8]	Preamble M Value used to indicate Preamble M
prem_w	[7:4]	Preamble W Value used to indicate Preamble W
prem_b	[3:0]	Preamble B Value used to indicate Preamble B

7.2.15 SLIMbus Configuration Control Register (SlmbConfig: 0x001E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				ext_sync_pulse_en			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						ready_sync	
Type	RO						R/W	
Default	0x00						0x1	

Register Field	Bit	Description
Reserved	[15:12]	
ext_sync_pulse_en	[11:8]	Enable for connecting HDMI Rx word select clock to the ext_presence_rate_clk i/p of SLIMbus IP
Reserved	[7:2]	
ready_sync	[1:0]	Number of slmb_clock clock cycles after negedge of audio sync pulse to next data launch

7.2.16 PLL Control Register 0 (PLLCtl0: 0x0020)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PLL_PRD				Reserved			PLL_FBD[8]
Type	R/W				RO			R/W
Default	0x4				0x00			0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PLL_FBD[7:0]							
Type	R/W							
Default	0x63							

Register Field	Bit	Description
PLL_PRD	[15:12]	Input divider setting Division ratio = (PRD3..0) + 1
Reserved	[11:9]	
PLL_FBD	[8:0]	Feedback divider setting Division ratio = (FBD8…0) + 1

7.2.17 PLL Control Register 1 (PLLCtl1: 0x0022)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				PLL_FRS		PLL_LBWS	
Type	RO				R/W		R/W	
Default	0x0				0x1		0x2	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Resvd	LFBREN	BYPCKEN	CKEN	Reserved		RESETB	PLL_EN
Type	RO	R/W	R/W	R/W	RO		R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0		0x0	0x0

Register Field	Bit	Description
Reserved	[15:12]	
PLL_FRS	[11:10]	Frequency range setting (post divider) for HSCK frequency 2'b00: 500MHz – 1GHz HSCK frequency 2'b01: 250MHz – 500MHz HSCK frequency 2'b10: 125 MHz – 250MHz HSCK frequency 2'b11: 62.5MHz – 125MHz HSCK frequency
PLL_LBWS	[9:8]	Loop bandwidth setting 2'b00: 25% of maximum loop bandwidth 2'b01: 33% of maximum loop bandwidth 2'b10: 50% of maximum loop bandwidth (default) 2'b11: maximum loop bandwidth
Reserved	[7]	
PLL_LFBREN	[6]	Lower Frequency Bound Removal Enable 1'b0: REFCLK toggling –> normal operation, REFCLK stops -> no oscillation 1'b1: REFCLK toggling -> normal operation, REFLCK stops -> free running PLL
PLL_BYPCKEN	[5]	Bypass clock enable 1'b0: Normal operation 1'b1: bypass mode, REFCLK is used instead of PLL_VCO output
PLL_CKEN	[4]	Clock enable 1'b0: clocks switched off (output LOW) 1'b1: clocks switched on
Reserved	[3:2]	
PLL_RESETB	[1]	PLL Reset 1'b0: Reset

		1'b1: Normal operation
PLL_EN	[0]	PLL Enable 1'b0: PLL off 1'b1: PLL on

7.2.18 PLL11 Control Register 0 (PLL11Ctl0: 0x0024)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PLL11_PRD				PLL11_FS		PLL11_BW	
Type	R/W				R/W		R/W	
Default	0x1				0x1		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PLL11_BYP	PLL11_FBD[6:0]						
Type	R/W	R/W						
Default	0x1	0x17						

Register Field	Bit	Description
PLL11_PRD	[15:12]	Input divider setting Division ratio = (PRD3..0) + 1
PLL11_FS	[11:10]	Clock output divider value 2'b00: Divide by 1 2'b01: Divide by 2 2'b10: Divide by 4 2'b11: Divide by 8
PLL11_BW	[9:8]	Bandwidth Setting 2'b00: Standard 2'b01: ½ of Standard or minimum 2'b10: ¼ of Standard or minimum 2'b11: 1/8 of Standard or minimum
PLL11_BYP	[7]	Bypass clock enable 1'b0: Normal operation 1'b1: bypass mode, REFCLK is used instead of PLL_VCO output
PLL11_FBD	[6:0]	Feedback divider setting Division ratio = (FBD6…0) + 1

7.2.19 PLL11 Control Register 1 (PLL11Ctl1: 0x0026)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LOCKDET	Reserved	SBRC_SRC		PLL11_DOEN	PLL11_CKEN	PLL11_IS[1:0]	
Type	RO	RO	R/W		R/W	R/W	R/W	
Default	0xX	0x0	0x0		0x0	0x0	0x2	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PLL11_OPD[7:0]							
Type	R/W							
Default	0x08							

Register Field	Bit	Description
LOCKDET	[15]	PLL11 Lock Detect Status
Reserved	[14]	Reserved
SBRC_SRC	[13:12]	SLIMbus Root Frequency Clock Source 2'b00: PLL11 based (default) 2'b01: HDMI Rx based

		2'b10: External Active Framer based 2'b11: Reserved
PLL11_DOEN	[11]	PLL11 output divider clock enable
PLL11_CKEN	[10]	PLL11 output clock enable
PLL11_IS	[9:8]	Current setting of charge pump 2'b00: IB x 0.5 2'b01: IB x 0.66 2'b10: IB x 1 (default) 2'b11: IB x 2
PLL11_OPD	[7:0]	Output divider setting Division ratio = (OPD7…0) + 1 OPD=0 bypasses this divider **This divider is used ONLY for SLIMbus clock and TESTMODE clock generation**

7.2.20 CSI-2TX Miscellaneous Control Register (CSI-2TX_MISC_CTRL: 0x0060)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CSI-2tx_wait_vsync
Type	RO							R/W
Default	0x0							0x0

Register Field	Bit	Description
Reserved	[15:1]	
CSI-2tx_wait_vsync	0	**CSI-2Tx Wait Control** 0: No wait before sending out video 1: CSI-2TX will wait for VSYNC before sending out video

7.3 IR Registers

7.3.1 IR Clock High Time Register 0 (IrHclk: 0x002C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					irhclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	irhclk							
Type	R/W							
Default	0x29							

Register Field	Bit	Description
Reserved	[15:11]	
irhclk	[10:0]	IR Clock High Time 0: Disable 1: 1 RefClk

		2: 2 RefClk ….

7.3.2 IR Clock Low Time Register 0 (IrLclk: 0x002E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					irlclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	irlclk							
Type	R/W							
Default	0x29							

Register Field	Bit	Description
Reserved	[15:11]	
Irlclk	[10:0]	IR Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk ….

7.3.3 IR Lead Code HMin Register (LCHmin: 0x0034)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				lchmin			
Type	RO				R/W			
Default	0x0				0x1			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	lchmin							
Type	R/W							
Default	0x50							

Register Field	Bit	Description
Reserved	[15:12]	
lchmin	[11:0]	IR Lead Code H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.4 IR Lead Code HMax Register (LCHmax: 0x0036)

Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved	lchmax
Type	RO	R/W
Default	0x0	0x1

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lchmax							
Type	R/W							
Default	0x64							

Register Field	Bit	Description
Reserved	[15:12]	
lchmax	[11:0]	IR Lead Code H Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.5 IR Lead Code LMin Register (LCLmin: 0x0038)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				lclmin			
Type	RO				R/W			
Default	0x0				0x0			

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lclmin							
Type	R/W							
Default	0xA3							

Register Field	Bit	Description
Reserved	[15:12]	
lclmin	[11:0]	IR Lead Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.6 IR Lead Code LMax Register (LCLmax: 0x003A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				lclmax			
Type	RO				R/W			
Default	0x0				0x0			

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lclmax							
Type	R/W							
Default	0xB7							

Register Field	Bit	Description
Reserved	[15:12]	
lclmax	[11:0]	IR Lead Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.7 IR Bit "H" HMin Register (BHHmin: 0x003C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhhmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhhmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
bhhmin	[11:0]	IR Bit H H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.8 IR Bit "H" H Max Register (BHHmax: 0x003E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhhmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhhmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
bhhmax	[11:0]	IR Bit H H Maximum Count 0: Not valid 1: 1 count 2: 2 count

		….

7.3.9 IR Bit "H" LMin Register (BHLmin: 0x0040)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhlmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	bhlmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
bhlmin	[11:0]	IR Bit H L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.10 IR Bit "H" LMax Register (BHLmax: 0x0042)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhlmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	bhlmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
bhlmax	[11:0]	IR Bit H L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.11 IR Bit "L" HMin Register (BLHmin: 0x0044)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				blhmin			

Type	RO				R/W			
Default	0x0				0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	blhmin							
Type	R/W							
Default	0x37							

Register Field	Bit	Description
Reserved	[15:12]	
blhmin	[11:0]	IR Bit L H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.12 IR Bit "L" HMax Register (BLHmax: 0x0046)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				blhmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	blhmax							
Type	R/W							
Default	0x4B							

Register Field	Bit	Description
Reserved	[15:12]	
blhmax	[11:0]	IR Bit L H Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.13 IR Bit "L" LMin Register (BLLmin: 0x0048)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bllmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	bllmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
bllmin	[11:0]	IR Bit L L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.14 IR Bit "L" LMax Register (BLLmax: 0x004A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bllmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bllmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
bllmax	[11:0]	IR Bit L L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.15 IR "END" HMin Register (EndHmin: 0x004C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				endhmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	endhmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	
endhmin	[11:0]	IR "END" H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.16 IR "END" HMax Register (EndHmax: 0x004E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				endhmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	endhmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	
endhmax	[11:0]	IR "END" H Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.17 IR Repeat Code LMin Register (RCLmin: 0x0050)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				rclmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	rclmin							
Type	R/W							
Default	0x4C							

Register Field	Bit	Description
Reserved	[15:12]	
rclmin	[11:0]	IR Repeat Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.18 IR Repeat Code LMax Register (RCLmax: 0x0052)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				rclmax			
Type	RO				R/W			

Default	0x0				0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	rclmax							
Type	R/W							
Default	0x60							

Register Field	Bit	Description
Reserved	[15:12]	
rclmax	[11:0]	IR Repeat Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

7.3.19 IR Control Register (IRCtl: 0x0058)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ir_ccode							
Type	R/W							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						ir_ccodem	Reserved
Type	RO						R/W	RO
Default	0x0						0x0	0x0

Register Field	Bit	Description
ir_ccode	[15:8]	IR Custom code TC358749XBG collects ir data only if the receive “custom code” match this ir_ccode (ir_ccodem=1’b0)
Reserved	[7:2]	
ir_ccodem	[1]	IR Custom Code Mask 0: Match 1: No Match (mask)
Reserved	[0]	

7.3.20 IR Data Register (IRData: 0x005A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ir_rccode							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	ir_rdata							
Type	RO							
Default	0x0							

Register Field	Bit	Description
ir_rccode	[15:8]	IR Receive custom code data
ir_rdata	[7:0]	IR Receive data

7.4 Miscellaneous Registers

7.4.1 CSI-2TX Miscellaneous Control Register (CSI-2TX_MISC_CTRL: 0x0060)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CSI-2tx_wait_vsync
Type	RO							R/W
Default	0x0							0x0

Register Field	Bit	Description
Reserved	[15:1]	
CSI-2tx_wait_vsync	0	**CSI-2Tx Wait Control** 0: No wait before sending out video 1: CSI-2TX will wait for VSYNC before sending out video

7.4.2 SLMB_AB_THRES (SLMB_AB_THRES: 0x0070)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	slmb_ab_thres						
Type	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:7]	
slmb_ab_thres	[6:0]	SLIMbus audio threshold For testing only.

7.4.3 I2S_IO_CTL (I2S_IO_CTL: 0x0072)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	Reserved						I2SCtl2	I2SCtl1
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:2]	
I2SCtl2	[1]	I2S Ctl2 CTL2 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins
I2SCtl1	[0]	I2S Ctl1 CTL1 of A_SCK, A_OSCK, A_WFS, A_SD_0, A_SD_1, A_SD_2 and A_SD_3 pins

7.4.4 IO Control0 Register 0 (IOCtl0: 0x0080)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						IRCtl2	IRCtl1
Type	RO						R/W	R/W
Default	0x0						0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	HPDOCtl2	HPDOCtl1	INTCtl2	INTCtl1	I2C_SDACtl2	I2C_SDACtl1	I2C_SCLCtl2	I2C_SCLCtl1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x1	0x0	0x1

Register Field	Bit	Description
Reserved	]1510]	These bits are write-able but the writes are ignored as these bits are not used anywhere.
IRCtl2	[9]	IR Current Drive Control {Ctl2, Ctl1}: **0: 1 mA** 1: 2 mA 2: 3 mA 3: 4 mA
IRCtl1	[8]	
HPDOCtl2	[7]	HPDO Current Drive Control {Ctl2, Ctl1}: **0: 1 mA** 1: 2 mA 2: 3 mA 3: 4 mA
HPDOCtl1	[6]	
INTCtl2	[5]	INT Current Drive Control {Ctl2, Ctl1}: **0: 1 mA** 1: 2 mA 2: 3 mA 3: 4 mA
INTCtl1	[4]	
I2C_SDACtl2	[3]	I2C_SDA Current Drive Control {Ctl2, Ctl1}: 0: 1 mA **1: 2 mA** 2: 3 mA 3: 4 mA
I2C_SDACtl1	[2]	
I2C_SCLCtl2	[1]	I2C_SCL Current Drive Control {Ctl2, Ctl1}: 0: 1 mA **1: 2 mA**
I2C_SCLCtl1	[0]	

		2: 3 mA 3: 4 mA

7.4.5 IO Control1 Register (IOCtl1: 0x0082)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					CECCpd	CECCpsel_1	CECCpsel_0
Type	R/W					R/W	R/W	R/W
Default	0x02					0x0	0x0	0x1
Bit	B7	B6	B5	B4	Bit	B7	B6	B5
Name	Reserved	DDC_SDACpd	DDC_SDACpsel_1	DDC_SDACpsel_0	Name	Reserved	DDC_SDACpd	DDC_SDACpsel_1
Type	R/O	R/W	R/W	R/W	Type	R/O	R/W	R/W
Default	0x0	0x1	0x0	0x0	Default	0x0	0x1	0x0

Register Field	Bit	Description
Reserved	[15:10]	These bits are write-able but the writes are ignored as these bits are not used anywhere.
CECCpd	[10]	CEC Cpd: 0 (Power Down); 1 (Active)
CECCpsel_1	[9]	CEC Threshold Voltage Settings: {Cpsel_1, Cpsel_0}: 0: VIH=1.7 ; VIL=1.1 1: VIH=1.7 ; VIL=1.4 2: VIH=2.1 ; VIL=1.7 3: VIH=2.4 ; VIL=2.0
CECCpsel_0	[8]	
Reserved	[7:6]	
DDC_SDACpd	[6]	DDC_SDA Cpd: 0 (Power Down); 1 (Active)
DDC_SDACpsel_1	[5]	DDC_SDA Threshold Voltage Settings: {Cpsel_1, Cpsel_0}: 0: VIH=1.7 ; VIL=1.1 1: VIH=1.7 ; VIL=1.4 2: VIH=2.1 ; VIL=1.7 3: VIH=2.4 ; VIL=2.0
DDC_SDACpsel_0	[4]	
Reserved	[3:2]	
DDC_SCLCpd	[2]	DDC_SCL Cpd: 0 (Power Down); 1 (Active)
DDC_SCLCpsel_1	[1]	DDC_SCL Threshold Voltage Settings: {Cpsel_1, Cpsel_0}: 0: VIH=1.7 ; VIL=1.1 1: VIH=1.7 ; VIL=1.4 2: VIH=2.1 ; VIL=1.7 3: VIH=2.4 ; VIL=2.0
DDC_SCLCpsel_0	[0]	

7.4.6 I2SPUDCTL (I2SPUDCTL: 0x0084)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		A_SD_3Pu	A_SD_3Pd	A_SD_2Pu	A_SD_2Pd	A_SD_1Pu	A_SD_1Pd
Type	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	A_SD_0Pu	A_SD_0Pd	A_WFSPu	A_WFSPd	A_SCKPu	A_SCKPd	A_OSCKPu	A_OSCKPd
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Default	0x0	0x1	0x1	0x0	0x1	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:4]	These bits are write-able but the writes are ignored as these bits are not used anywhere.
A_SD_3Pu	[13]	A_SD_3 Pull Up
A_SD_3Pd	[12]	A_SD_3 Pull Down
A_SD_2Pu	[11]	A_SD_2 Pull Up
A_SD_2Pd	[10]	A_SD_2 Pull Down
A_SD_1Pu	[9]	A_SD_1 Pull Up
A_SD_1Pd	[8]	A_SD_1 Pull Down
A_SD_0Pu	[7]	A_SD_0 Pull Up
A_SD_0Pd	[6]	A_SD_0 Pull Down
A_WFSPu	[5]	A_WFS Pull Up
A_WFSPd	[4]	A_WFS Pull Down
A_SCKPu	[3]	A_SCK Pull Up
A_SCKPd	[2]	A_SCK Pull Down
A_OSCKPu	[1]	A_OSCK Pull Up
A_OSCKPd	[0]	A_OSCK Pull Down

7.4.7 I2S_IR Control Register (I2SIRCtl: 0x7082)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					I2SWFSInv	IRInv	I2SSCKInv
Type	R/W					R/W	R/W	R/W
Default	0x00					0	0x0	0

Register Field	Bit	Default	Description
Reserved	[15:3]	0x0	These bits used by IR Control Register
I2SWFSInv	2	0x0	**I2SWFSInv** (Option to use inverted or non-inverted I2S Word Select Clock) 1: Invert I2S WFS Polarity
IRInv	1	0x0	**IRInv** (Option to use inverted or non-inverted polarity) 1: Invert IR Polarity
I2SSCKInv	0	0x0	**I2SSCKInv** (Option to use inverted or non-inverted I2S Shift Clock) 1: Invert I2S Shift Clock Polarity

7.5 CSI-2 Registers

7.5.1 CSI-2 Tx PHY

7.5.1.1 Clock Lane DPHY TX Control register (CLW_DPHYCONTTX: 0x0100)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CLW_CAP1	CLW_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		CLW_LPTXCURR1EN	CLW_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 7-3 Clock Lane DPHY TX Control register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
CLW_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Clock Lane
CLW_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Clock Lane (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
CLW_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for clock Lane.

Register Field	Bit	Default	Description
CLW_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for clock Lane. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

7.5.1.2 Data Lane 0 DPHY TX Control register (D0W_DPHYCONTTX:0x0104)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D0W_CAP1	D0W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved	Reserved	D0W_LPTXCURR1EN	D0W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 7-4 Data Lane 0 DPHY TX Control register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D0W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 0.
D0W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 0. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]

Register Field	Bit	Default	Description
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Data output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
D0W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
D0W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

7.5.1.3 Data Lane 1 DPHY TX Control Register (D1W_DPHYCONTTX: 0x0108)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D1W_CAP1	D1W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D1W_LPTXCURR1EN	D1W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 7-5 Data Lane 1 DPHY TX Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D1W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 1.

Register Field	Bit	Default	Description
D1W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 1. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 7ps.
Reserved	[3:2]	0x0	
D1W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1.
D1W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

7.5.1.4 Data Lane 2 DPHY TX Control Register (D2W_DPHYCONTTX: 0x010C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D2W_CAP1	D2W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D2W_LPTXCURR1EN	D2W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 7-6 Data Lane 2 DPHY TX Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D2W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 2.
D2W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 2. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
D2W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2.
D2W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

7.5.1.5 Data Lane 3 DPHY TX Control Register (D3W_DPHYCONTTX: 0x0110)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D3W_CAP1	D3W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D3W_LPTXCURR1EN	D3W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 7-7 Data Lane 3 DPHY TX Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D3W_CAP1	[9]	0x1	Selection bit 1 of different HSTX output capacitors for Data Lane 3.
D3W_CAP0	[8]	0x0	Selection bit 0 of different HSTX output capacitors for Data Lane 3. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	0x0	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	0x0	
D3W_LPTXCURR1EN	[1]	0x1	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3.
D3W_LPTXCURR0EN	[0]	0x0	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

7.5.1.6 Data Lane 0 DPHY RX Control Register (D0W_DPHYCONTRX: 0x0124)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		D0W_CUTRSEL	D0W_LPRXVTHLO	Reserved			

				W				
Type	RO	RO	R/W	R/W	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-8 Data Lane 0 DPHY RX Control Register

Register Field	Bit	Default	Description
Reserved	[15:6]	0x0	
D0W_CUTRSEL	[5]	0x0	LPRXVTHLOW CUTR value select for Data Lane 0 1: LPRXVTHLOW value is set by CUTR cell 0: LPRXVTHLOW value is set by D0W_LPRXVTHLOW
D0W_LPRXVTHLOW	[4]	0x0	LPRX input threshold select for Data Lane 0 1: LPRX input threshold is low 0: LPRX input threshold is high (default)
Reserved	[3:0]	0x0	

7.5.1.7 DPHY RX Common Control Register (COM_DPHYCONTRX: 0x0138)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						LPRXCALRES	LPRXCALEN
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 7-9 DPHY RX Common Control Register

Register Field	Bit	Default	Description
Reserved	[15:2]	0x0	
LPRXCALRES	[1]	0x0	LPRX Calibration Reset 0: Not Reset 1: Reset high When this bit is set to “1” and a Reset is implemented, this bit must remain “1” for 500ns or longer.

Register Field	Bit	Default	Description
LPRXCALEN	[0]	0x0	LPRX Calibration Enable 0: Calibration Switch OFF 1: Calibration Switch ON When this bit is set to “1” and Calibration is implemented, this bit must remain at “1” for 500ns or longer.

7.5.1.8 Clock Lane DPHY Control Register (CLW_CNTRL: 0x0140)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CLW_CNTRL	
Type	RO						R/W	
Default	0x00						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CLW_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 7-10 Clock Lane DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
CLW_CNTRL	[9:8]	0x0	Reserved
Reserved	[7:1]	0x0	
CLW_LaneDisable	[0]	0x0	Force Lane Disable for Clock Lane. 1’b1: Force Lane Disable 1’b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

7.5.1.9 Data Lane 0 DPHY Control Register (D0W_CNTRL: 0x0144)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D0W_CNTRL	
Type	RO						R/W	
Default	0x00						0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	Reserved	D0W_LaneDisable
Type	RO	R/W
Default	0x00	0

Table 7-11 Data Lane 0 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D0W_CNTRL	[9:8]	0x0	Reserved
Reserved	[7:1]	0x0	
D0W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

7.5.1.10 Data Lane 1 DPHY Control Register (D1W_CNTRL: 0x0148)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D1W_CNTRL	
Type	RO						R/W	
Default	0x00						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D1W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 7-12 Data Lane 1 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D1W_CNTRL	[9:8]	0x0	Reserved
Reserved	[7:1]	0x0	
D1W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

7.5.1.11 Data Lane 2 DPHY Control Register (D2W_CNTRL: 0x014C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D2W_CNTRL	
Type	RO						R/W	
Default	0x00						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D2W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 7-13 Data Lane 2 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D2W_CNTRL	[9:8]	0x0	Reserved
Reserved	[7:1]	0x0	
D2W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 2. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

7.5.1.12 Data Lane 3 DPHY Control Register (D3W_CNTRL: 0x0150)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D3W_CNTRL	
Type	RO						R/W	
Default	0x00						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D3W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 7-14 Data Lane 3 DPHY Control Register

Register Field	Bit	Default	Description

Register Field	Bit	Default	Description
Reserved	[15:10]	0x0	
D3W_CNTRL	[9:8]	0x0	Reserved
Reserved	[7:1]	0x0	
D3W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 3. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable. When SCANTESTMODE=1, this register is disabled. When SCANMODE=0, this register is always enabled.

7.5.2 CSI-2 Tx PPI

7.5.2.1 PPI STARTCNTRL (STARTCNTRL: 0x0204)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							START
Type	RO	RO	RO	RO	RO	RO	RO	W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[31:1]	
START	[0]	START control bit of PPI-TX function. By writing 1 to this bit, PPI starts function. 0: Stop function. (default). Writing 0 is invalid and the bit can be set to zero by system reset only. 1: Start function. The following registers are set to appropriate value before starting any transmission by START bit in STARTCTRL register. Once START bit is set to high, the change of the register bits does not affect to function. In order to change the values, toggle SysCtr[CTxRst] is necessary.

7.5.2.2 PPI STATUS (PPISTATUS: 0x0208)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							BUSY
Type	RO	RO	RO	RO	RO	RO	RO	R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description

Reserved	[31:1]	
BUSY	[0]	After writing 1 to the START bit in the STARTCNTRL register, this bit is set until SysCtr[CTxRst] is asserted. 0: Not Busy. (default) 1: Busy.

7.5.2.3 LINEINITCNT (LINEINITCNT: 0x0210)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LINEINITCNT[15:8]							
Type	R/W							
Default	0x20							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LINEINITCNT[7:0]							
Type	R/W							
Default	0x8E							

Register Field	Bit	Description
Reserved	[31:16]	
LINEINITCNT	[15:0]	Line Initialization Wait Counter This counter is used for line initialization. **Set this register before setting [STARTCNTRL].START = 1.** MIPI specification requires that the slave device needs to observe LP-11 for 100 us and ignore the received data before the period at initialization time. The count value depends on HFCLK and the value needs to be set to achieve more than 100 us. The counter starts after the START bit of the STARTCNTRL register is set. The Master device needs to output LP-11 for 100 us in order for the slave device to observe LP-11 for the period. For example, in order to set 100 us when the period of HFCLK is 12 ns, the counter value should be more than 8333.3 = 0x208D (100 us / 12 ns). Default is 0x208E.

7.5.2.4 LPTXTIMECNT (LPTXTIMECNT: 0x0214)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					LPTXTIMECNT[10:8]		
Type	RO					R/W		
Default	0x00					0x0		

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LPTXTIMECNT[7:0]							
Type	R/W							
Default	0x01							

Register Field	Bit	Description
Reserved	[15:11]	
LPTXTIMECNT	[10:0]	SYSLPTX Timing Generation Counter The counter generates a timing signal for the period of LPTX. This counter is counted using the HSByteClk (the Main Bus clock), and the value of (setting + 1) * HSByteClk Period becomes the period LPTX. Be sure to set the counter to a value greater than 50 ns.

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.5 TCLK_HEADERCNT (TCLK_HEADERCNT: 0x0218)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TCLK_ZEROCNT[7:0]							
Type	R/W							
Default	0x01							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	TCLK_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Register Field	Bit	Description
TCLK_ZEROCNT	[15:8]	**TCLK_ZERO Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PRE + TCLK-ZERO for Clock Lane, this counter is used. This counter is counted by HSBYTECLk. Set this register in order to set the minimum time (TCLK-PRE + TCLK-ZERO) to a value greater than 300 ns. The actual value is ((1 to 2) + (TCLK_ZEROCNT + 1)) x HSByteClkCycle + (PHY output delay). The PHY output delay is about (0 to 1) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) x MIPIBitClk cycle in the BitClk conversion.
Reserved	[7]	

Register Field	Bit	Description
TCLK_PREPARECNT	[6:0]	**TCLK_PREPARE Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PREPARE for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set TCLK-PREPARE period that is greater than 38 ns but less than 95 ns. Calculating formula (TCLK_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.6 TCLK_TRAILCNT (TCLK_TRAILCNT: 0x021C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	TCLKTRAILCNT[7:0]							
Type	R/W							
Default	0x01							

Register Field	Bit	Description
Reserved	[15:8]	
TCLK_TRAILCNT	[7:0]	**TCLK_TRAIL Counter** This counter is used for Clock Lane control in Master mode. In order to satisfy the timing parameter about TCLK-TRAIL and TEOT for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set TCLK-TRAIL to a value greater than 60 ns and TEOT to a value less than 105 ns + 12 x UI The actual value is (TCLK_TRAILCNT + (1 to 2)) x HSByteClkCycle + (2+(1 to 2)) * HSBYTECLKCycle - (PHY output delay). The PHY output delay is about (0 to 1) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) x MIPIBitClk cycle in the BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.7 THS_HEADERCNT (THS_HEADERCNT: 0x0220)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	THS_ZEROCNT[6:0]						

Type	RO	R/W						
Default	0	0x01						
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	Reserved	THS_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Register Field	Bit	Description
THS_ZEROCNT	[14:8]	**THS_ZERO Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE + THS-ZERO for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register to set the (THS-PREPARE + THS-ZERO) period, which should be greater than (145 ns + 10 x UI) results. The actual value is ((1 to 2) + 1 + (TCLK_ZEROCNT + 1) + (3 to 4)) x ByteClk cycle + HSByteClk x (2+(1 to 2)) +(PHY delay). The PHY output delay is about (1 to 2) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (8+(5 to 6)) x MIPIBitClk cycle in BitClk conversion.
Reserved	[7]	
THS_PREPARECNT	[6:0]	**THS_PREPARE Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set the THS-PREPARE period, which should be greater than (40 ns + 4xUI) and less than (8 5 ns + 6xUI) results. Calculating Formula: (THS_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.8 TWAKEUP (TWAKEUP: 0x0224)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TWAKEUPCNT[15:8]							
Type	R/W							
Default	0x4E							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	TWAKEUPCNT[7:0]							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[31:16]	
TWAKEUPCNT	[15:0]	**TWAKEUP Counter** This counter is used to exit ULPS state. Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state. This counter is counted by the unit of LPTXTIMECNT.

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.9 TCLK_POSTCNT (TCLK_POSTCNT: 0x0228)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					TCLK_POSTCNT[10:8]		
Type	RO					R/W		
Default	0x00					0x2		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TCLK_POSTCNT[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[15:11]	
TCLK_POSTCNT	[10:0]	**TCLK_POST Counter** This counter is used for Clock Lane control in Master mode. This counter is counted by the HSByteClk. Set a value greater than (60 ns + 52 x UI) results. The actual value is ((1 to 2) + (TCLK_POSTCNT + 1)) x HSByteClk cycle + (1) x HSBYTECLK cycle.

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.10 THS_TRAILCNT (THS_TRAILCNT: 0x022C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				THS_TRAILCNT[3:0]			
Type	RO				R/W			
Default	0x0				0x2			

Register Field	Bit	Description
Reserved	[15:4]	
THS_TAILCNT	[3:0]	**THS_TRAIL Counter** This counter is used for Data Lane control in Master mode. This counter is counted by HSBYTECLK. Set a value greater 8 x UI or (60 ns + 4 x UI) and less than TEOT which is 105 ns + 12 x UI results. The actual value is (1 + THS_TRAILCNT) x ByteClk cycle + ((1 to 2) + 2) x HSBYTECLK cycle - (PHY output delay). The PHY output delay is about (1 to 2) x HSByteClkCycle in ByteClk conversion performed during RTL simulation and is about (8+(5 to 6)) x MIPIBitClk cycle in BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.11 HSTXVREGCNT (HSTXVREGCNT: 0x0230)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	HSTXVREGCNT[15:8]							
Type	R/W							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HSTXVREGCNT[7:0]							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
HSTXVREGCNT	[15:0]	TX Voltage Regulator setup Wait Counter This counter is used for all lanes of HSTXVREG commonly. Counter value is counted by HFCLK. The counter starts when START bit is set. After the counter is counted up, PPI-TX can change the line from LP mode to HS mode. If the counter value is set to zero, there is no wait by the counter. Recommended counter value will be decided by evaluation. It was determined that a value of 200 ns max in the ELDEC TEG skew evaluation results (5/21/2009) is sufficient. LINEINCNT is 100 us, so any value less than that will not affect the value of this counter. The value 1 us is used in the example setting.

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.12 HSTXVREGEN (HSTXVREGEN: 0x0234)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							

Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	Reserved			D3M_HSTXVREGEN	D2M_HSTXVREGEN	D1M_HSTXVREGEN	D0M_HSTXVREGEN	CLM_HSTXVREGEN
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[15:5]	
D3M_HSTXVREGEN	[4]	Voltage regulator enable for HSTX Data Lane 3. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D2M_HSTXVREGEN	[3]	Voltage regulator enable for HSTX Data Lane 2. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D1M_HSTXVREGEN	[2]	Voltage regulator enable for HSTX Data Lane 1. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D0M_HSTXVREGEN	[1]	Voltage regulator enable for HSTX Data Lane 0. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
CLM_HSTXVREGEN	[0]	Voltage regulator enable for HSTX Clock Lane. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.13 TXOPTIONCNTRL (TXOPTIONCNTRL: 0x0238)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO

Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	Reserved							CONTCLK MODE
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[15:1]	
CONTCLKMODE	[0]	**Set Continuous Clock Mode** Writing "1" to this bit will set the Clock Lane to the Continuous Clock mode regardless of the PPI interface signal and will maintain the Clock Lane output. 0: Non-continuous clock mode. Transitions into the LP11 state in coordination with the Data Lane operation. 1: Continuous clock mode. Maintains the Clock Lane output regardless of the Data Lane operation.

This bit can be rewritten when [STATUS].BUSY is set.
Set this register before setting [STARTCNTRL].START = 1. Do not change this register after START = 1 is set.

7.5.2.14 BTACNTRL1 (BTACNTRL1: 0x023C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved					TXTAGOCNT[10:8]		
Type	RO	RO	RO	RO	RO	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	B16
Name	TXTAGOCNT[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	B8
Name	Reserved					RXTASURECNT[10:8]		
Type	RO	RO	RO	RO	RO	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	RXTASURECNT[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	1	0	0	0

Table 6-29 BTACNTRL1

Register Field	Bit	Default	Description
Reserved	[31:27]	0x0	
TXTAGOCNT	[26:16]	0x8	The TTA-GO period (LP-00 drive period) when drive privileges are released by BTA is set by the setting of this counter. The period for driving LP-00 for the TTA-GO period is 4 x (TXTAGOCNT + 1) x (HSByteClk cycle). Set so that the TTA-GO period (4 x TLPX) described in the MIPI D-PHY specifications results.
Reserved	[15:11]	0x0	
RXTASURECNT	[10:0]	0x8	The timing for starting driving of LP-00 in the TTA-SURE period when drive privileges are obtained by BTA is set by the setting of this counter. The drive start timing is (RXTASURECNT + (3 or 2)) x (HSByteClk cycle) cycle. Set so as to be within the TTA-SURE period (Min TLPX, Max 2 x TLPX) range described in the MIPI D-PHY specifications.

Set this register before setting [STARTCNTRL].START = 1.

7.5.2.15 PPI D0S ATMR Register (D0S_ATMR: 0x0244)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					D0S_ATMREN	D0S_ATMR	
Type	RO					R/W	R/W	
Default	0x00					0	0	

Table 7-15 PPI D0S ATMR Register

Register Field	Bit	Default	Description

Register Field	Bit	Default	Description
Reserved	[31:3]	0x0	
D0S_ATMREN	2	0x0	D0S_ATMREN: Analog timer function enable for Data Lane 0 in LPRX. 0: analog timer function off (default) 1:analog timer function on
D0S_ATMR	[1:0]	0x0	D0S_ATMR[1:0] Selection of different delay times for tuning of Analog Timer for Data Lane 0 in LPRX. (0,0): Bypass mode (0,1): delay = D1 (1,0): delay = D2 (default) (1,1): delay = D3

Note: Set this register before setting [STARTCNTRL].START = 1.

7.5.2.16 CLS_PRE Register (CLS_PRE: 0x0280)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CLS_PREEN	Reserved		CLS_PREFLG	Reserved		CLS_SETPRE	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CLS_SETPRE							
Type	R/W							
Default	0x00							

Register Field	Bit	Description

Reserved	[31:16]	
CLS_PREEN	15	**CLS_SETPREEN** CLS_SETPRE Register bit Enable. CLS_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of CLS_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
CLS_PREFLG	12	**CLS_PREFLG** Flag indicating counter value SETPRE has been reached for Clock Lane. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
CLS_SETPRE	[9:0]	**CLS_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Clock Lane. 10'b00_0000_0000: (Temporary default)

7.5.2.17 D0S_PRE Register (D0S_PRE: 0x0284)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D0S_PREEN	Reserved		D0S_PREFLG	Reserved		D0S_SETPRE	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D0S_SETPRE							
Type	R/W							
Default	0x00							

Register Field	Bit	Description

Reserved	[31:16]	
D0S_PREEN	15	**D0S_SETPREEN** D0S_SETPRE Register bit Enable. D0S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D0S_PREFLG	12	**D0S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 0. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D0S_SETPRE	[9:0]	**D0S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 0. 10'b00_0000_0000: (Temporary default)

7.5.2.18 D1S_PRE Register (D1S_PRE: 0x0288)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D1S_PREEN	Reserved		D1S_PREFLG	Reserved		D1S_SETPRE	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D1S_SETPRE							
Type	R/W							
Default	0x00							

Register Field	Bit	Description

Reserved	[31:16]	
D1S_PREEN	15	**D1S_SETPREEN** D1S_SETPRE Register bit Enable. D1S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D1S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D1S_PREFLG	12	**D1S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 1. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D1S_SETPRE	[9:0]	**D1S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 1. 10'b00_0000_0000: (Temporary default)

7.5.2.19 D2S_PRE Register (D2S_PRE: 0x028C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D2S_PREEN	Reserved		D2S_PREFLG	Reserved		D2S_SETPRE	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D2S_SETPRE							
Type	R/W							
Default	0x00							

Register Field	Bit	Description

Reserved	[31:16]	
D2S_PREEN	15	**D2S_SETPREEN** D2S_SETPRE Register bit Enable. D2S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D2S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D2S_PREFLG	12	**D2S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 2. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D2S_SETPRE	[9:0]	**D2S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 2. 10'b00_0000_0000: (Temporary default)

7.5.2.20 D3S_PRE Register (D3S_PRE: 0x0290)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D3S_PREEN	Reserved		D3S_PREFLG	Reserved		D3S_SETPRE	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	D3S_SETPRE							
Type	R/W							
Default	0x00							

Register Field	Bit	Description

Reserved	[31:16]	
D3S_PREEN	15	**D3S_SETPREEN** D3S_SETPRE Register bit Enable. D3S_SETPRE is normally controlled by PPI internally, but when enable is asserted, the value of D3S_SETPRE in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D3S_PREFLG	12	**D3S_PREFLG** Flag indicating counter value SETPRE has been reached for Data Lane 3. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPRE. 1: Counter has reached to the value SETPRE.
Reserved	[11:10]	
D3S_SETPRE	[9:0]	**D3S_SETPRE[9:0]** Bit Counter value when PREFLG should be activated for Data Lane 3. 10'b00_0000_0000: (Temporary default)

7.5.2.21 CLS_PREP Register (CLS_PREP: 0x02A0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CLS_PREPEN	Reserved		CLS_PREPFLG	Reserved		CLS_SETPREP	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CLS_SETPREP							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
CLS_PREPEN	15	**CLS_SETPREPEN** CLS_SETPREP Register bit Enable. CLS_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of CLS_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
CLS_PREPFLG	12	**CLS_PREPFLG** Flag indicating counter value SETPREP has been reached for Clock Lane. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
CLS_SETPREP	[9:0]	**CLS_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Clock Lane. 10'b00_0000_0000: (Temporary default)

7.5.2.22 D0S_PREP Register (D0S_PREP: 0x02A4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D0S_PREPEN	Reserved		D0S_PREPFLG	Reserved		D0S_SETPREP	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D0S_SETPREP							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
D0S_PREPEN	15	**D0S_SETPREPEN** D0S_SETPREP Register bit Enable. D0S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D0S_PREPFLG	12	**D0S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 0. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D0S_SETPREP	[9:0]	**D0S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 0. 10'b00_0000_0000: (Temporary default)

7.5.2.23 D1S_PREP Register (D1S_PREP: 0x02A8)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D1S_PREPEN	Reserved		D1S_PREPFLG	Reserved		D1S_SETPREP	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D1S_SETPREP							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
D1S_PREPEN	15	**D1S_SETPREPEN** D1S_SETPREP Register bit Enable. D1S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D1S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D1S_PREPFLG	12	**D1S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 1. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D1S_SETPREP	[9:0]	**D1S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 1. 10'b00_0000_0000: (Temporary default)

7.5.2.24 D2S_PREP Register (D2S_PREP: 0x02AC)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D2S_PREPEN	Reserved		D2S_PREPFLG	Reserved		D2S_SETPREP	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D2S_SETPREP							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
D2S_PREPEN	15	**D2S_SETPREPEN** D2S_SETPREP Register bit Enable. D2S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D2S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D2S_PREPFLG	12	**D2S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 2. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D2S_SETPREP	[9:0]	**D2S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 2. 10'b00_0000_0000: (Temporary default)

7.5.2.25 D3S_PREP Register (D3S_PREP: 0x02B0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D3S_PREPEN	Reserved		D3S_PREPFLG	Reserved		D3S_SETPREP	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D3S_SETPREP							
Type	R/W							
Default	0x00							

Register Field	Bit	Description

Reserved	[31:16]	
D3S_PREPEN	15	**D3S_SETPREPEN** D3S_SETPREP Register bit Enable. D3S_SETPREP is normally controlled by PPI internally, but when enable is asserted, the value of D3S_SETPREP in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D3S_PREPFLG	12	**D3S_PREPFLG** Flag indicating counter value SETPREP has been reached for Data Lane 3. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETPREP. 1: Counter has reached to the value SETPREP.
Reserved	[11:10]	
D3S_SETPREP	[9:0]	**D3S_SETPREP[9:0]** Bit Counter value when PREPFLG should be activated for Data Lane 3. 10'b00_0000_0000: (Temporary default)

7.5.2.26 CLS_ZERO Register (CLS_ZERO: 0x02C0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CLS_ZEROEN	Reserved		CLS_ZEROFLG	Reserved		CLS_SETZERO	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CLS_SETZERO							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
CLS_ZEROEN	15	**CLS_SETZEROEN** CLS_SETZERO Register bit Enable. CLS_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of CLS_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
CLS_ZEROFLG	12	**CLS_ZEROFLG** Flag indicating counter value SETZERO has been reached for Clock Lane. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
CLS_SETZERO	[9:0]	**CLS_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Clock Lane. 10'b00_0000_0000: (Temporary default)

7.5.2.27 D0S_ZERO Register (D0S_ZERO: 0x02C4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D0S_ZEROEN	Reserved		D0S_ZEROFLG	Reserved		D0S_SETZERO	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D0S_SETZERO							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
D0S_ZEROEN	15	**D0S_SETZEROEN** D0S_SETZERO Register bit Enable. D0S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D0S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D0S_ZEROFLG	12	**D0S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 0. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D0S_SETZERO	[9:0]	**D0S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 0. 10'b00_0000_0000: (Temporary default)

7.5.2.28 D1S_ZERO Register (D1S_ZERO: 0x02C8)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D1S_ZEROEN	Reserved		D1S_ZEROFLG	Reserved		D1S_SETZERO	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D1S_SETZERO							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
D1S_ZEROEN	15	**D1S_SETZEROEN** D1S_SETZERO Register bit Enable. D1S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D1S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D1S_ZEROFLG	12	**D1S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 1. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D1S_SETZERO	[9:0]	**D1S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 1. 10'b00_0000_0000: (Temporary default)

7.5.2.29 D2S_ZERO Register (D2S_ZERO: 0x02CC)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D2S_ZEROEN	Reserved		D2S_ZEROFLG	Reserved		D2S_SETZERO	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D2S_SETZERO							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
D2S_ZEROEN	15	**D2S_SETZEROEN** D2S_SETZERO Register bit Enable. D2S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D2S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D2S_ZEROFLG	12	**D2S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 2. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D2S_SETZERO	[9:0]	**D2S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 2. 10'b00_0000_0000: (Temporary default)

7.5.2.30 D3S_ZERO Register (D3S_ZERO: 0x02D0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	D3S_ZEROEN	Reserved		D3S_ZEROFLG	Reserved		D3S_SETZERO	
Type	R/W	RO		RO	RO		R/W	
Default	0x0	0x0		0x0	0x0		0x0	

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D3S_SETZERO							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[31:16]	
D3S_ZEROEN	15	**D3S_SETZEROEN** D3S_SETZERO Register bit Enable. D3S_SETZERO is normally controlled by PPI internally, but when enable is asserted, the value of D3S_SETZERO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
Reserved	[14:13]	
D3S_ZEROFLG	12	**D3S_ZEROFLG** Flag indicating counter value SETZERO has been reached for Data Lane 3. It stops the counter. If wirite to this bit, there is no affect. Read is valid. 0: Counter has not reached to the value SETZERO. 1: Counter has reached to the value SETZERO.
Reserved	[11:10]	
D3S_SETZERO	[9:0]	**D3S_SETZERO[9:0]** Bit Counter value when ZEROFLG should be activated for Data Lane 3. 10'b00_0000_0000: (Temporary default)

7.5.2.31 PPI_CLRFLG Register (PPI_CLRFLG: 0x02E0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D3_CLRFLGEN	D3CLRFLG
Type	RO						R/W	R/W
Default	0x0						0x0	0x0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D2_CLRFLGEN	D2CLRFLG	D1_CLRFLGEN	D1CLRFLG	D0_CLRFLGEN	D0CLRFLG	CL_CLRFLGEN	CLCLRFLG
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description

Reserved	[31:6]	
D3_CLRFLGEN	9	**D3_CLRFLGEN** D3_CLRFLG Register bit Enable. D3_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of D3_CLRFLG in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D3_CLRFLG	8	**D3_CLRFLG** Flag indicating counter value SETPRE has been reached for Data Lane 3. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D2_CLRFLGEN	7	**D2_CLRFLGEN** D2_CLRFLG Register bit Enable. D2_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of D2_CLRFLG in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D2_CLRFLG	6	**D2_CLRFLG** Flag indicating counter value SETPRE has been reached for Data Lane 2. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D1_CLRFLGEN	5	**D1_CLRFLGEN** D1_CLRFLG Register bit Enable. D1_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of D1_CLRFLG in the register is valid and the value from PPI block is invalid. 0 Disable. (default) 1: Enable.
D1_CLRFLG	4	**D1_CLRFLG** Flag indicating counter value SETPRE has been reached for Data Lane 1. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D0_CLRFLGEN	3	**D0_CLRFLGEN** D0_CLRFLG Register bit Enable. D0_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of D0_CLRFLG in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D0_CLRFLG	2	**D0_CLRFLG** Flag indicating counter value SETPRE has been reached for Data Lane 0. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY.

		(default)
CL_CLRFLGEN	1	**CL_CLRFLGEN** CL_CLRFLG Register bit Enable. CL_CLRFLG is normally controlled by PPI internally, but when enable is asserted, the value of CL_CLRFLG in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
CL_CLRFLG	0	**CL_CLRFLG** Flag indicating counter value SETPRE has been reached for Clock Lane. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)

7.5.2.32 PPI_CLRSIPO Register (PPI_CLRSIPO: 0x02E4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D3_CLRSIPOEN	D3CLRSIPO
Type	RO						R/W	R/W
Default	0x0						0x0	0x0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	D2_CLRSIPOEN	D2CLRSIPO	D1_CLRSIPOEN	D1CLRSIPO	D0_CLRSIPOEN	D0CLRSIPO	CL_CLRSIPOEN	CLCLRSIPO
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description

Reserved	[31:6]	
D3_CLRSIPOEN	9	**D3_CLRSIPOEN** D3_CLRSIPO Register bit Enable. D3_CLRSIPO is normally controlled by PPI internally, but when enable is asserted, the value of D3_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D3_CLRSIPO	8	**D3_CLRSIPO** Flag indicating counter value SETPRE has been reached for Data Lane 3. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D2_CLRSIPOEN	7	**D2_CLRSIPOEN** D2_CLRSIPO Register bit Enable. D2_CLRSIPO is normally controlled by PPI internally, but when enable is asserted, the value of D2_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D2_CLRSIPO	6	**D2_CLRSIPO** Flag indicating counter value SETPRE has been reached for Data Lane 2. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D1_CLRSIPOEN	5	**D1_CLRSIPOEN** D1_CLRSIPO Register bit Enable. D1_CLRSIPO is normally controlled by PPI internally, but when enable is asserted, the value of D1_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D1_CLRSIPO	4	**D1_CLRSIPO** Flag indicating counter value SETPRE has been reached for Data Lane 1. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
D0_CLRSIPOEN	3	**D0_CLRSIPOEN** D0_CLRSIPO Register bit Enable. D0_CLRSIPO is normally controlled by PPI internally, but when enable is

		asserted, the value of D0_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
D0_CLRSIPO	2	**D0_CLRSIPO** Flag indicating counter value SETPRE has been reached for Data Lane 0. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)
CL_CLRSIPOEN	1	**CL_CLRSIPOEN** CL_CLRSIPO Register bit Enable. CL_CLRSIPO is normally controlled by PPI internally, but when enable is asserted, the value of CL_CLRSIPO in the register is valid and the value from PPI block is invalid. 0: Disable. (default) 1: Enable.
CL_CLRSIPO	0	**CL_CLRSIPO** Flag indicating counter value SETPRE has been reached for Clock Lane. It stops the counter. This bit is valid when TESTMODEREGEN is enabling. 0: TIMER is running. 1: Asynchronous signal to clear the 3 counter flags. Synchronized with HSCK in D-PHY. (default)

7.5.3 CSI-2 Tx Control Register

7.5.3.1 CSI-2 Configuration Read Register (CSI-2_CONTROL: 0x040C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CSI-2_mode	Reserved	PrToEn	TaToEn	LrxToEn	HtxToEn	CntDis	EccDis
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	1	0	1	1	1	1	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TxMd	CrcDis	HsCkMd	Reserved		NOL[1:0]		EoTDis
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CSI-2_mode	15	**CSI-2 Mode Selection** 1: CSI-2 Mode 0: Reserved
Reserved	14	Reserved
PrToEn	13	**PR_TO_EN** 0: Disables the PR_TO timer. 1: Enables the PR_TO timer.
TaToEn	12	**TA_TO_EN** 0: Disables the TA_TO timer. 1: Enables the TA_TO timer.
LrxToEn	11	**LPRX_TO_EN** 0: Disables the LRX-H_TO timer. 1: Enables the LRX-H _TO timer.
HtxToEn	10	**HSTX_TO_EN** 0: Disables the HTX_TO timer. 1: Enables the HTX_TO timer.
CntDis	9	**CONTENTION_DIS** This bit disables contention detection.
EccDis	8	**ECC_DISABLE** This bit sets operation for when there are multiple-bit ECC errors in the received data. If multiple-bit ECC errors are detected, the ECC Error multi bit (bit 9) bit of the CSI-2_RXERR register is asserted to “1” regardless of this bit’s setting. In the case of ECC single-bit errors, the setting of this bit has no effect on the operation. Single-bit errors can be corrected, so the corrected data can be stored in the Receive FIFO regardless of this bit’s setting. At this time, the ECC Error single bit (bit 8) bit of the CSI-2_RXERR is asserted to “1”, and the settings of the CSI-2_ERR_HALT, and CSI-2_ERR_INTENA registers are valid. 0: If there are multiple-bit ECC errors in the received data, subsequent processes including the fetching of data from the peripheral interface are terminated and wait for the LP Stop state. Loading to the Receive FIFO of the corresponding packets is not performed. 1: Even if multiple-bit ECC errors are detected in the received data, subsequent processes including the fetching of data from the peripheral interface continue. Either the packet in which multiple bit ECC errors were detected is loaded into the Receive FIFO or the corresponding package waits for a valid Data Type. If the Data Type is

		invalid, the CSI-2 Data Type no recognized (bit 11) bit of the CSI-2_RXERR register is set to “1” and the packet is discarded. If a valid Data Type is recognized, the packet is stored in the Receive FIFO. In the case of a long packet, processing continues up to the reception of the data payload.
TxMd	7	**TXMODE** 0: Low power transfer is performed to Tx. 1: High-Speed data transfer is performed to Tx.
CrcDis	6	**CRC_DISABLE** Operation for when a CRC error was found in the received data is set. (For long packets only) 0: CRC checking of received long packets is performed. If CRC errors exist in the received data, the CRC Error bit (bit 10) of the CSI-2_RXERR register is asserted to “1”. Transfers to the Receive FIFO for the received data are performed. 1: CRC checking of received long packets is not performed. Even if there are CRC errors in the received data, no notification is made to the CSI-2_RXERR register. The CRC errors are ignored and transfers to the Receive FIFO for the received data are performed.
HsCkMd	5	**HSCLOCKMODE** 0: Operation is in the discontinuous clock mode. 1: Operation is in the continuous clock mode.
Reserved	[4:3]	
NOL	[2:1]	**NOL** This field specifies the number of HS lanes. This field is also used as the LP Lane Enable setting. Data Lane 0 is used as the Enable for LP communication and ULPS. Data Lane 1 or higher is used as the Enable for ULPS. This setting can only be made during initial setup or during reset. 00: Only Data Lane 0 is used. 01: Data Lanes 0 and 1 are used. 10: Data Lanes from 0 to 2 are used. 11: Data Lanes 0 to 3 are used.
EoTDis	0	**EOT_DISABLE** 0: The EOT packet is automatically granted at the end of HS transfer then is transmitted. 1: The EOT packet is not automatically granted at the end of HS transfer and is not transmitted.

Only indirect writing, i.e. write to CSI-2_CONFW Register is possible.

7.5.3.2 CSI-2 STATUS Register (CSI-2_STATUS: 0x0410)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					WSync	TxAct	RxAct
Type	RO					RO	RO	RO
Default	0xX					0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	RxAF	RxAE	RxEm	Reserved				Hlt
Type	RO	RO	RO	RO				RO
Default	0	1	0	0xX				0

Register Field	Bit	Default	Description

Register Field	Bit	Default	Description
Reserved	[15:11]	X	
WSync	10	0	**Wait Sync Signal** This bit indicates that the CSI-2-TX module is waiting for a particular Sync signal
TxAct	9	0	**Transmitter Active** This bit indicates that the CSI-2-TX module is in the Transmit mode.
RxAct	8	0	**Receiver Active** This bit indicates that the CSI-2-TX module is in the Receive mode.
RxAF	7	0x0	**FIFO_ALMOSTFULL** This bit indicates that the Receive FIFO is almost full (has less than 3 empty slots).
RxAE	6	0x1	**FIFO ALMOSTEMPTY** This bit indicates that the Receive FIFO is almost empty (has less than 2 entries).
RxEm	5	0x0	**FIFO EMPTYn** This bit indicates that the Receive FIFO is **not** empty.
Reserved	[4:1]	X	
Hlt	0	0	**Halted** The CSI-2-TX module is stopped by either an error or a pause request.

7.5.3.3 CSI-2_INT Register (CSI-2_INT: 0x0414)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					IntAck	Reserved	
Type	RO					RO	RO	
Default	0x00					0	0x00	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				IntHlt	IntEr	IntRxEr	IntAkEr
Type	RO				RO	RO	RO	RO
Default	0x00				0	0	0	0

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	

Register Field	Bit	Default	Description
IntAk	18	0x0	**INT_ACK** This bit indicates that the Acknowledge trigger has been received.
Reserved	[17:4]	0x0	
IntHlt	3	0x0	**INT_HALTED** The CSI-2-TX module was stopped by an error or a pause request.
IntEr	2	0x0	**INT_CSI-2_ERR** An interrupt was requested by a CSI-2_ERR register error.
IntRxEr	1	0x0	**INT_CSI-2_RXERR** An interrupt was requested by a CSI-2_RXERR register error.
IntAkEr	0	0x0	**INT_CSI-2_ACKERR** An interrupt was requested by a CSI-2_ACKERR register error.

Each bit can indirectly clear a register value either when “1” is written to the bit of each corresponding CSI-2_INT_CLR register.

7.5.3.4 CSI-2_INT_ENA Register (CSI-2_INT_ENA: 0x0418)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					IEnAk	Reserved	
Type	RO					RO	RO	
Default	0x00					0	0x0	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				IEnHlt	IEnEr	IEnRxEr	IEnAkEr
Type	RO				RO	RO	RO	RO
Default	0x0				0	0	0	0

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	
IEnAk	18	0x0	**INTENA_ACK** This bit enables interrupt notification by INT_ACK sources.
Reserved	[17:4]	0x0	
IEnHlt	3	0x0	**INTENA_HALTED** This bit enables interrupt notification by INT_HALTED sources.
IEnEr	2	0x0	**INTENA_CSI-2_ERR**

Register Field	Bit	Default	Description
			This bit enables interrupt notification by INT_CSI-2_ERR sources.
IEnRxEr	1	0x0	**INTENA_CSI-2_RXERR** This bit enables interrupt notification by INT_CSI-2_RXERR sources.
IEnAkEr	0	0x0	**INTENA_CSI-2_ACKERR** This bit enables interrupt notification by INT_CSI-2_ACKERR sources.

Only indirect writing, i.e. write to CSI-2_CONFW with [Addr] = 0x06.

7.5.3.5 CSI-2 Command Read Data FIFO Register (CSI-2CMD_RDFIFO: 0x0430)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	RDDATA[31:24]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	RDDATA[23:16]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	RDDATA[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	RDDATA[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-16 CSI-2 Command Read Data FIFO Register

Register Field	Bit	Default	Description
RDDATA	[31:0]	0x0	**RDDATA** Data received from the peripheral interface via the CSI-2 link is written to this register.

The data received via a CSI-2 link was written to this register.

7.5.3.6 CSI-2_ACKERR Register (CSI-2_ACKERR: 0x0434)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ACKERR_REPORT[15:8]							

Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACKERR_REPORT[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-29 ACKERR_REPORT Register

Register Field	Bit	Default	Description
Reserved	[31:16]	0x0	
ACKERR_REPORT	[15:0]	0x0	**ACKERR_REPORT** The content of the Acknowledge packet with report of the last error received is held.

The content of the CSI-2_ACKERR register is cleared when the register is read.

7.5.3.7 CSI-2_ACKERR_INTENA Register (CSI-2_ACKERR_INTENA: 0x0438)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CSI-2_ACKERR_INTENA[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CSI-2_ACKERR_INTENA[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-17 CSI-2_ACKERR_INTENA Register

Register Field	Bit	Default	Description
Reserved	[31:16]	0x0	
CSI-2_ACKERR_INTENA	[15:0]	0x0	**CSI-2_ACKERR_INTENA** This field sets the generation of interrupts when an acknowledge packet with error report is received. Setting each bit in this field enables generation of the CSI-2_ACKERR_INT interrupt which corresponds to the CSI-2_ACKERR register error.

Only indirect writing, i.e. write to CSI-2_CONFW with [Addr] = 0x0E.

7.5.3.8 CSI-2_ACKERR_HALT Register (CSI-2_ACKERR_HALT: 0x043C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CSI-2_ACKERR_HALT[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CSI-2_ACKERR_HALT[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-18 CSI-2_ACKERR_HALT Register

Register Field	Bit	Default	Description
Reserved	[31:16]	0x0	
CSI-2_ACKERR_HALT	[15:0]	0x0	**CSI-2_ACKERR_HALT** This field controls operation of the CSI-2-TX module when an acknowledge packet with error report is received. The CSI-2-TX module halts command processes when an error is received for which the corresponding bit in the CSI-2_ACKERR_INTENA and CSI-2_ACKERR_HALT registers is set.

Only indirect writing, i.e. write to CSI-2_CONFW with [Addr] = 0x0F.

7.5.3.9 CSI-2_RXERR Register (CSI-2_RXERR: 0x0440)

Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved			TATo	RxHTo	Reserved	FOvrFlw	Reserved
Type	RO			RO	RO	RO	RO	RO
Default	0			0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		InCmplTx	Reserved	DTErr	CRCErr	ECCSErr	ECCMErr
Type	RO		RO	RO	RO	RO	RO	RO
Default	0		0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	LPCtlErr	Reserved	LPSyncErr	EscErr	Reserved		
Type	RO	RO	RO	RO	RO	RO		
Default	0	0	0	0	0	0		

Table 6-29 CSI-2_RXERR Register

Register Field	Bit	Default	Description

Reserved	[31:21]	0x0	
TATo	20	0x0	**TA_TO** This bit indicates direction change acknowledgement timeouts.
RxHTo	19	0x0	**LRX-H_TO** This bit indicates LP-RX host processor timeouts.
Reserved	18	0x0	
FOvrFlw	17	0x0	**FIFO_OVERFLOW** This bit indicates Receive FIFO overflows.
Reserved	[16:14]	0x0	
InCmplTx	13		Incomplete Tx
Reserved	12	0x0	
DTErr	11		CSI-2 packet Data Type is not reconized
CRCErr	10		CRC Error
ECCSErr	9		ECC Error, Single bit
ECCMErr	8		ECC Error, Multi- bits
Reserved	7	0x0	
CtlErr	6		False Control Error
Reserved	5		
LPSyncErr	4		LP Sync Error
EscErr	3		Escape Mode Entry Error
Reserved	[2:0]	0x0	

The content of the CSI-2_RXERR register is cleared when the register is read.

7.5.3.10 CSI-2_RXERR_INTENA Register (CSI-2_RXERR_INTENA: 0x0444)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved			CSI-2_RXERR_INTENA[20:16]				
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	CSI-2_RXERR_INTENA[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CSI-2_RXERR_INTENA[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-19 CSI-2_RXERR_INTENA Register

Register Field	Bit	Default	Description
Reserved	[31:21]	0x0	
CSI-2_RXERR_INTENA	[20:0]	0x0	**CSI-2_RXERR_INTENA** This field controls generation of interrupts when the CSI-2_RXERR register is notified of an error. Each bit in this field enables generation of the CSI-2_RXERR_INT interrupt which corresponds to the CSI-2_RXERR register error.

Only indirect writing, i.e. write to CSI-2_CONFW with [Addr] = 0x11.

7.5.3.11 CSI-2_RXERR_HALT Register (CSI-2_RXERR_HALT: 0x0448)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved			CSI-2_RXERR_HALT[20:16]				
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CSI-2_RXERR_HALT[15:8]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CSI-2_RXERR_HALT[7:0]							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-20 CSI-2_RXERR_HALT Register

Register Field	Bit	Default	Description
Reserved	[31:21]	0x0	
CSI-2_RXERR_HALT	[20:0]	0x0	**CSI-2_RXERR_HALT** This field controls CSI-2-TX operation for when an error has been reported to the CSI-2_RXERR register. The CSI-2-TX module stops command processing when it receives an error corresponding to the set bits in the CSI-2_RXERR_INTENA and CSI-2_RXERR_HALT registers.

Only indirect writing, i.e. write to CSI-2_CONFW with [Addr] = 0x12.

7.5.3.12 CSI-2_ERR Register (CSI-2_ERR: 0x044C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						InEr	WCEr
Type	RO						RO	RO
Default	0x00						0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	SynTo	RxFRdEr	TeEr	QUnk	QWrEr	HTxTo	HTxBrk	Cntn
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
InEr	9	0x0	**INTERNAL_ERROR** This bit indicates that another internal error occurred.
WCEr	8	0x0	**WC_ERROR** This bit indicates that more bytes than expected were received from the PDIF. Because distinguishing the current data from the next payload data of continuous transfers is difficult when the last payload data is 4-byte aligned, this error is not detected.
SynTo	7	0x0	**SYNC_TO** This bit indicates that a synchronous wait timeout occurred.
RxFRdEr	6	0x0	**RXFIFO_RDERR** This bit indicates that an empty Receive FIFO was read.
TeEr	5	0x0	**TE_ERROR** This bit indicates that the peripheral interface did not transmit the tearing trigger the CSI-2-TX module is expecting.
QUnk	4	0x0	**CQ_UNKNOWN** This bit indicates that an unknown command or incorrect parameter was detected by the command queue.
QWrEr	3	0x0	**CQ_WRERR** This bit indicates that Write access to a full command queue occurred.
HTxTo	2	0x0	**HTX_TO** This bit indicates that a High-Speed TX timeout occurred.
HTxBrk	1	0x0	**HSTX_BROKEN** This bit indicates that the byte stream was disrupted during High-Speed transfer.
Cntn	0	0x0	**CONTENTION** This bit indicates that a contention was detected during lower power transfer.

The content of the CSI-2_ERR register is cleared by reading it out.

7.5.3.13 CSI-2_ERR_INTENA (CSI-2_ERR_INTENA: 0x0450)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CSI-2_ERR_INTENA[9:8]	
Type	RO						RO	

Default	0x00						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CSI-2_ERR_INTENA[7:0]							
Type	RO							
Default	0xbf							

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
CSI-2_ERR_INTENA	[9:0]	0xbf	**CSI-2_ERR_INTENA** This field controls interrupt generation for when an error has been reported to the CSI-2_ERR register. Generation of the CSI-2_ERR_INT interrupt which corresponds to the CSI-2_ERR register error is enabled.

Only indirect writing, i.e. write to CSI-2_CONFW with [Addr] = 0x14.

7.5.3.14 CSI-2_ERR_HALT Register (CSI-2_ERR_HALT: 0x0454)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CSI-2_ERR_HALT[9:8]	
Type	RO						RO	
Default	0x00						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CSI-2_ERR_HALT[7:0]							
Type	RO							
Default	0xbf							

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
CSI-2_ERR_HALT	[9:0]	0xbf	**CSI-2_ERR_HALT** This field controls CSI-2-TX operation for when an error is reported to the CSI-2_ERR register. The CSI-2-TX module stops command processing when it receives an error corresponding to the set bits in the CSI-2_ERR_INTENA and CSI-2_ERR_HALT registers.

Only indirect writing, i.e. write to CSI-2_CONFW with [Addr] = 0x15.

7.5.3.15 CSI-2 Configuration Register (CSI-2_CONFW: 0x0500)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	MODE			Address				
Type	WO	WO	WO	WO	WO	WO	WO	WO

Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	B16
Name	DATA [23:16]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	B8
Name	DATA[15:8]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	DATA[7:0]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MODE	[31:29]	**Set or Clear AddrReg (register specified in Address field) Bits** 3'b101: Set Register Bits in AddReg as indicated in DATA field 3'b110: Clear Register Bits in AddReg as indicated in DATA field Others: Reserved
Address	[28:24]	**Address Field** 0x03: CSI-2_Control, 0x040C, Register 0x06: CSI-2_INT_ENA, 0418, Register 0x0E: CSI-2_ACKERR_INTENA, 0x0438, Register 0x0F: CSI-2_ACKERR_HALT, 0x043C, Register 0x11: CSI-2_RXERR_INTENA, 0x0444 Register 0x12: CSI-2_RXERR_ HALT, 0x0448, Register 0x14: CSI-2_ERR_INTENA, 0x0450, Register 0x15: CSI-2_ERR_ HALT, 0x0454, Register Others: Reserved
DATA	[23:0]	**DATA Field** When location DATA[n] is set to '1', the corresponding bit at AddrReg[n] will be cleared or set depending on MODE bits described above. Multiples bits can be set simultaneously

Note: Write to CSI-2_CONFW Register results to changes in corresponding bit changed in AddrReg Register.

7.5.3.16 CSI-2 LP Command (CSI-2_LPCMD: 0x0500 *)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	LP Command							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	1	1	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[23:16]							

Type	WO							
Default	0xXX							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[15:8]							
Type	WO							
Default	0xXX							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LANE_ENA					LP_Code		
Type	WO	WO	WO	WO	WO	WO		
Default	0	0	0	0	0	0		

Note: This command share the register CSI-2_CONFW. It is in LP command mode when [31:24] = 0x30

Register Field	Bit	Default	Description
LPCommand	[31:24]	0x0	**LP Command Mode Selection** 8'h30: Set Register Bits to this value to enable LP Command mode Others: Reserved
Reserved	[23:8]	0x0	Reserved
LANE_ENA	[7:3]	0x0	**LANE Enable Field** This Lane Enable is only used by LPC_CODE 000 (ULPS transition) and 001 (LP Stop transition). Select the following Lanes within the range of Lanes set to "Enable" by CSI-2_CONTROL[NOL]. Do not set ULPS transition and LP Stop transition for Lanes that have not been set to "Enable" by the NOL bit. LANE_ENA[3]: Select Clock Lanes LANE_ENA[4]: Select Lane 0 LANE_ENA[5]: Select Lane 1 LANE_ENA[6]: Select Lane 2 LANE_ENA[7]: Select Lane 3
LP_CODE	[2:0]	0x0	000: The Lane indicated by LANE_ENA transitions to ULPS (the ultra low power state). 001: The Lane indicated by LANE_ENA transitions to the LP stop state. 010: A remote application reset trigger is transmitted to Lane 0. Then, Lane 0 returns to the LP stop state. The state of other Lanes is not affected. 011: Bus direction change (BTA) is executed on Lane 0. After BTA, Lane 0 returns to the LP Stop state. Other Lanes are not affected. Others: Reserved

Note: Setting 0x0500 = 0x300000F8 with put the clock lane and 4 data lanes into ULPS mode.
While sending any packet during ULPS mode will cause CSI-2 link to exit ULPS mode.

7.5.3.17 CSI-2_RESET Register (CSI-2_RESET: 0x0504)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			RstRxF	Reserved		RstCnf	RstMdl
Type	RO			WO	RO		WO	WO
Default	0			0	X		0	0

Register Field	Bit	Default	Description
Reserved	[31:5]	0x0	
RstRxF	4	0x0	**RST_RXFIFO** 0: Operation is not affected. 1: The Receive FIFO is reset.
Reserved	[3:2]	0xX	
RstCnf	1	0x0	**RST_CONF** 0: Operation is not affected. 1: Reset Configures registers only.
RstMdl	0	0x0	**RST_MODULE** Do not set this bit to "1". Perform a hardware reset when a CSI-2TX block reset is necessary. Use this bit when resetting the sub modules inside this block (CSI-2 layer). The PHY layer or the application layer blocks are not reset. 0: Operation is not affected. 1: Reset CSI-2 Logic only.

7.5.3.18 CSI-2_INT_CLR Register (CSI-2_INT_CLR: 0x050C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					ICrAk	Reserved	
Type	RO					WO	RO	
Default	0					0	0	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				ICrHlt	ICrEr	ICrRxEr	ICrAkEr
Type	RO				WO	WO	WO	WO
Default	0				0	0	0	0

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	
ICrAk	18	0x0	**INTCLR_ACK** 0: Operation is not affected. 1: The INT_ACK interrupt is cleared.

Register Field	Bit	Default	Description
Reserved	[17:4]	0x0	
ICrHlt	3	0x0	**INTCLR_HALTED** 0: Operation is not affected. 1: The INT_HALTED interrupt is cleared.
ICrEr	2	0x0	**INTCLR_CSI-2_ERR** 0: Operation is not affected. 1: The INT_CSI-2_ERR interrupt is cleared.
ICrRxEr	1	0x0	**INTCLR_CSI-2_RXERR** 0: Operation is not affected. 1: The INT_CSI-2_RXERR interrupt is cleared.
ICrAkEr	0	0x0	**INTCLR_CSI-2_ACKERR** 0: Operation is not affected. 1: The INT_CSI-2_ACKERR interrupt is cleared.

7.5.3.19 CSI-2_START (CSI-2_START: 0x0518)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[7:1]							Strt
Type	RO	RO	RO	RO	RO	RO	RO	WO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[31:1]	
Strt	0	**CSI-2 Transmission START** 0: The clock is not supplied to modules other than CONIF. 1: The clock is supplied to all modules. When “1” is written to this bit, the clock is supplied to modules other than the CSI-2-TX CONIF. To start CSI-2-TX operation, set this bit to “1” after a reset is performed. This bit must be set to “1” even when accessing registers other than CSI-2_START. Once this bit is set to “1”, writing of “0” is not allowed. Perform a reset to change this bit from “1” to “0”.

7.6 CEC Control Registers

7.6.1 CEC Clock High Time Register 0 (CecHclk: 0x0028)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					cechclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	cechclk							
Type	R/W							
Default	0x90							

Register Field	Bit	Description
Reserved	[15:11]	
cechclk	[10:0]	CEC Clock High Time 0: Disable 1: 1 RefClk 2: 2 RefClk ….

7.6.2 CEC Clock Low Time Register 0 (CecLclk: 0x002A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					ceclclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ceclclk							
Type	R/W							
Default	0x90							

Register Field	Bit	Description
Reserved	[15:11]	
ceclclk	[10:0]	CEC Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk ….

7.6.3 CEC Enable Register (CECEN: 0x0600)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CECEN
Type	RO							R/W
Default	0x0							0x0

Table 7-21 CEC Enable Register

Register Field	Bit	Description
Reserved	[15:1]	
CECEN	0	**CEC operation** 0: Disable 1: Enable

7.6.4 CEC Logical Address Register (CECADD: 0x0604)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CECADD[15:8]							
Type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CECADD[7:0]							
Type	R/W							
Default	0x0							

Table 7-22 CEC Logical Address Register

Register Field	Bit	Description
CECADD[15:0]	[15:0]	**Specify logical address assigned to CEC** Each bit corresponds to individual address, therefore multiple addresses can be assigned to CEC logic

7.6.5 CEC Reset Register (CECRST: 0x0608)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CECRST
Type	RO							R/W
Default	0x0							0x0

Table 7-23 CEC Reset Register

Register Field	Bit	Description
Reserved	[15:1]	Reserved
CECRST	[0]	**CEC soft reset** 0: Disable 1: Enable Setting this bit to "1" affects the following: - Reception: Stops immediately. The received data is discarded. -Transmission (including the CEC line): Stops immediately. - Registers: The following registers are initialized. (CECADD, CECREN, CECRCR1, CECRCR2, CECRCR3,CECTEN, CECTCR, CECRSTAT, CECTSTAT, CECRBUF01-16, CECTBUF01-16, CECRCTR)

7.6.6 CEC Receive Enable (CECREN: 0x060C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CECREN
Type	RO							R/W
Default	0x0							0x0

Table 7-24 CEC Receive Enable Register

Register Field	Bit	Description
Reserved	[15:1]	Reserved
CECREN	[0]	**CEC reception enable** 0: Disable 1: Enable

7.6.7 CEC Receive Control Register 1 (CECRCTL1: 0x0614)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							CECACKDIS
Type	RO							R/W
Default	0x0							0x0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved		CECHNC[1:0]		Reserved	CECLNC[2:0]		
Type	RO		R/W		RO	R/W		
Default	0x0		0x0		0x0	0x0		
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	CECMIN[2:0]			Reserved	CECMAX[2:0]		
Type	RO	R/W			R	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B6
Name	Reserved	CECDAT[2:0]			CECTOUT[1:0]		CECRIHLD	CECOTH
Type	RO	R/W			R/W		R/W	R/W
Default	0x0	0x0			0x0		0x0	0x0

Table 7-25 CEC Receive Control Register 1

Register Field	Bit	Description
Reserved	[31:25]	Reserved
CECACKDIS	[24]	Enable ACK transmission 0: Disable 1: Enable
Reserved	[23:22]	Reserved
CECHNC	[21:20]	Number of consecutive cycles sampling logical '1' for noise cancellation 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles

Register Field	Bit	Description
Reserved	[19]	Reserved
CECLNC	[18:16]	Number of consecutive cycles sampling logical '0' for noise cancellation 000: 1 cycle 001: 2 cycles 100: 3 cycles 100: 4 cycles 111: 8 cycles
Reserved	[15]	Reserved
CECMIN	[14:12]	The minimum time to to detect valid bit value. Error is detected when signal changes earlier than the minimum value 000: 2.05ms 001: 2.05ms+1cycle 010: 2.05ms+2cycles 011: 2.05ms+3cycles 100: 2.05ms-1cycle 101: 2.05ms-2cycles 110: 2.05ms-3cycles 111: 2.05ms-4cycles
Reserved	[11]	Reserved
CECMAX	[10:8]	The maximum time to detect valid bit value. Error is detected when signal does not change within the maximum time 000: 2.75ms 001: 2.75ms+1cycle 010: 2.75ms+2cycles 011: 2.75ms+3cycles 100: 2.75ms-1cycle 101: 2.75ms-2cycles 110: 2.75ms-3cycles 111: 2.75ms-4cycles
Reserved	[7]	Reserved
CECDAT	[6:4]	Time to detect CEC signal as valid (0 or 1) 000: 1.05ms 001: 1.05ms+2cycles 010: 1.05ms+4cycles 011: 1.05ms+6cycles 100: 1.05ms-2cycles 101: 1.05ms-4cycles 110: 1.05ms-6cycles 111: Reserved
CECTOUT	[3:2]	Number of cycles to determine timeout 00: 1 bit cycle 01: 2 bit cycles 10: 3 bit cycles 11: Reserved
CECRIHLD	[1]	Suspend CEC receive error interrupt 0: Disable 1: Enable
CECOTH	[0]	For Testing only. Enable the CEC reception when address does not match 0: Disable

Register Field	Bit	Description
		1: Enable

7.6.8 CEC Receive Control Register 2 (CECRCTL2: 0x0618)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	CECSWAV3[2:0]			Reserved	CECSWAV2[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	CECSWAV1[2:0]			Reserved	CECSWAV0[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		

Table 7-26 CEC Receive Control Register 2

Register Field	Bit	Description
Reserved	[15]	Reserved
CECSWAV3	[14:12]	Maximum time to detect start bit 000: 4.7ms 001: 4.7ms+1cycle 010: 4.7ms+2cycles 011: 4.7ms+3cycles 100: 4.7ms+4cycles 101: 4.7ms+5cycles 110: 4.7ms+6cycles 111: 4.7ms+7cycles
Reserved	[11]	Reserved
CECSWAV2	[10:8]	Minimum time to detect start bit 000: 4.3ms 001: 4.3ms-1cycle 010: 4.3ms-2cycles 011: 4.3ms-3cycles 100: 4.3ms-4cycles 101: 4.3ms-5cycles 110: 4.3ms-6cycles 111: 4.3ms-7cycles
Reserved	[7]	Reserved
CECSWAV1	[6:4]	Maximum time to detect start bit rising 000: 3.9ms 001: 3.9ms+1cycle 010: 3.9ms+2cycles 011: 3.9ms+3cycles 100: 3.9ms+4cycles 101: 3.9ms+5cycles 110: 3.9ms+6cycles 111: 3.9ms+7cycles
Reserved	[3]	Reserved
CECSWAV0	[2:0]	Minimum time to detect start bit rising 000: 3.5ms 001: 3.5ms-1cycle 010: 3.5ms-2cycles 011: 3.5ms-3cycles 100: 3.5ms-4cycles

Register Field	Bit	Description
		101: 3.5ms-5cycles 110: 3.5ms-6cycles 111: 3.5ms-7cycles

7.6.9 CEC Receive Control Register 3 (CECRCTL3: 0x061C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved	CECWAV3[2:0]			Reserved	CECWAV2[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved	CECWAV1[2:0]			Reserved	CECWAV0[2:0]		
Type	RO	R/W			R	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B6**
Name	Reserved			CECACKEI	CECMINEI	CECMAXEI	CECRSTEI	CECWAVEI
Type	RO			R/W	R/W	R/W	R/W	R/W
Default	0x0			0x0	0x0	0x0	0x0	0x0

Table 7-27 CEC Receive Control Register 3

Register Field	Bit	Description
Reserved	[31:23]	Reserved
CECWAV3	[22:20]	The latest rising timing of logical 0 000: 1.7ms 001: 1.7ms+1cycle 010: 1.7ms+2cycles 011: 1.7ms+3cycles 100: 1.7ms+4cycles 101: 1.7ms+5cycles 110: 1.7ms+6cycles 111: 1.7ms+7cycles
Reserved	[19]	Reserved
CECWAV2	[18:16]	The fastest rising timing of a logical 0 000: 1.3ms 001: 1.3ms-1cycle 010: 1.3ms-2cycles 011: 1.3ms-3cycles 100: 1.3ms-4cycles 101: 1.3ms-5cycles 110: 1.3ms-6cycles 111: 1.3ms-7cycles
Reserved	[15]	Reserved
CECWAV1	[14:12]	The latest rising timing of logical 1 000: 0.8ms

Register Field	Bit	Description
		001: 0.8ms+1cycle 010: 0.8ms+2cycles 011: 0.8ms+3cycles 100: 0.8ms+4cycles 101: 0.8ms+5cycles 110: 0.8ms+6cycles 111: 0.8ms+7cycles
Reserved	[11]	Reserved
CECWAV0	[10:8]	The fastest rising of a logical 1 000: 0.4ms 001: 0.4ms-1cycle 010: 0.4ms-2cycles 111: 0.4ms-3cycles 100: 0.4ms-4cycles 101: 0.4ms-5cycles 110: 0.4ms-6cycles 111: 0.4ms-7cycles
Reserved	[7:5]	Reserved
CECACKEI	[4]	ACK collision error interrupt enable 0: Disable 1: Enable
CECMINEI	[3]	Minimum timing error detection interrupt enable 0: Disable 1: Enable
CECMAXEI	[2]	Maximum timing error detection interrupt enable 0: Disable 1: Enable
CECRSTEI	[1]	Start bit interrupt enable 0: Disable 1: Enable
CECWAVEI	[0]	Waveform error interrupt enable 0: Disable 1: Enable

7.6.10 CEC Transmit Enable Register (CECTEN: 0x0620)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						CECTBusy	CECTEN
Type	RO						RO	R/W
Default	0x0						0x0	0x0

Table 7-28 Audio Data Double Word Count Register 2

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTBusy	[1]	CEC transmit state (read only) 0: idle 1: active
CECTEN	[0]	CEC transmission control 0: Disable 1: Enable

7.6.11 CEC Transmit Control Register (CECTCTL: 0x0628)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved	CECSTRS[2:0]			Reserved	CECSPRD[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	CECDTRS[2:0]			CECDPRD[3:0]			
Type	RO	R/W			R/W			
Default	0x0	0x0			0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			CECBRD	CECFREE[3:0]			
Type	RO			R/W	R/W			
Default	0x0			0x0	0x0			

Table 7-29 CEC Transmit Control Register

Register Field	Bit	Description
Reserved	[31:23]	Reserved
CECSTRS	[22:20]	Rising cycle time of the start bit – between the default values and 0-7 cycles 000: default value (~ 3.7ms) 001: default value – 1 cycle 010: default value – 2 cycles 011: default value – 3 cycles 100: default value – 4 cycles 101: default value – 5 cycles 110: default value – 6 cycles 111: default value – 7 cycles
Reserved	[19]	Reserved
CECSPRD	[18:16]	Start bit cycle time 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle

		110: RV –6cycle 111: RV –7cycle
Reserved	[15]	Reserved
CECDTRS	[14:12]	Rising cycle time of data bit 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle 110: RV –6cycle 111: RV –7cycle
CECDPRD	[11:8]	Data bit cycle time 0000: RV 1000: RV – 8 cycles 0001: RV – 1 cycle 1001: RV – 9 cycles 0010: RV – 2 cycles 1010: RV – 10 cycles 0011: RV – 3 cycles 1011: RV – 11 cycles 0100: RV – 4 cycles 1100: RV – 12 cycles 0101: RV – 5 cycles 1101: RV – 13 cycles 0110: RV – 6 cycles 1110: RV – 14 cycles 0111: RV – 7 cycles 1111: RV – 15 cycles
Reserved	[7:5]	Reserved
CECBRD	[4]	Broadcast transmit enable 1'b0: disable 1'b1: enable
CECFREE	[3:0]	Number of cycles for checking the line to be inactive before the start of transmission 0000: 1-bit cycle 1000: 9 bit cycle 0001: 2 bit cycle 1001: 10 bit cycle 0010: 3 bit cycle 1010: 11 bit cycle 0011: 4 bit cycle 1011: 12 bit cycle 0100: 5 bit cycle 1100: 13 bit cycle 0101: 6 bit cycle 1101: 14 bit cycle 0110: 7 bit cycle 1110: 15 bit cycle 0111: 8 bit cycle 1111: 16 bit cycle

7.6.12 CEC Receive Interrupt Status Register (CECRSTAT: 0x062C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	CECRIWA	CECRIOR	CECRIACK	CECRIMIN	CECRIMAX	CECRISTA	CECRIEND
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x2	0x0	0x0

Table 7-30 CEC Receive Interrupt Status Register

Register Field	Bit	Description

Reserved	[15:7]	Reserved
CECRIWA	[6]	CEC Waveform error interrupt flag
CECRIOR	[5]	Receive buffer full flag
CECRIACK	[4]	ACK collision detection flag
CECRIMIN	[3]	Bit cycle time is less than minimum time flag
CECRIMAX	[2]	Bit cycle time is greater than maximum time flag
CECRISTA	[1]	Start bit detection flag
CECRIEND	[0]	Reception of CEC message with EOM

7.6.13 CEC Transmit Interrupt Status Register (CECTSTAT: 0x0630)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved			CECTIUR	CECTIACK	CECTIAL	CECTIEND	Reserved
Type	RO			RO	RO	RO	RO	RO
Default	0x0			0x0	0x0	0x0	0x0	0x0

Table 7-31 Interrupt Flag Register

Register Field	Bit	Description
Reserved	[15:5]	Reserved
CECTIUR	[4]	Transmission is completed and the transmit buffer is empty
CECTIACK	[3]	ACK error detection flag
CECTIAL	[2]	Arbitration loss flag (“0” is detected while transmit “1”)
CECTIEND	[1]	Data block transmission completion flag
Reserved	[0]	Reserved

7.6.14 CEC Receive Buffer Registers (01-16) (CECRBUF01-16: 0x0634-0x0670)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CECRACK	CECEOM
Type	RO						RO	RO
Default	0x0						0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CECRBYTE[7:0]							
Type	RO							
Default	0x0							

Table 7-32 CEC Receive Buffer Registers (01-16)

Register Field	Bit	Description
Reserved	[15:10]	Reserved
CECRACK	[9]	ACK bit received
CECEOM	[1]	EOM bit received
CECRBYTE	[7:0]	CEC byte received

7.6.15 CEC Transmit Buffer Registers (01-16) (CECTBUF01-16: 0x0674-0x06B0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							CECTEOM
Type	RO							R/W
Default	0x0							0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CECTBYTE[7:0]							
Type	R/W							
Default	0x0							

Table 7-33 CEC Transmit Buffer Registers (01-16)

Register Field	Bit	Description
Reserved	[15:9]	Reserved
CECTEOM	[8]	EOM bit value to be transmitted
CECTBYTE	[7:0]	Byte data to be transmitted

7.6.16 CEC Receive Byte Counter Register (CECRCTR: 0x06B4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved			CECRCTR[4:0]				
Type	RO			RO				
Default	0x0			0x0				

Table 7-34 Interrupt Flag Register

Register Field	Bit	Description
Reserved	[15:5]	Reserved
CECRCTR	[4:0]	Numbers of bytes received

7.6.17 CEC Interrupt Enable Register (CECIMSK: 0x06C0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						CECTIM	CECRIM
Type	RO						R/W	R/W
Default	0x0						0x0	0x0

Table 7-35 CEC Interrupt Enable Register

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTIM	[1]	CEC Transmit status interrupt enable 1'b0: disable 1'b1: enable
CECRIM	[0]	CEC Receive status interrupt enable 1'b0: disable 1'b1: enable

7.6.18 CEC Interrupt Clear Register (CECICLR: 0x06CC)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						CECTClr	CECRClr
Type	RO						WO	WO
Default	0x0						0x0	0x0

Table 7-36 CEC Interrupt Enable Register

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTIM	[1]	Host writes "1" to this bit to clear CEC Transmit status interrupt
CECRIM	[0]	Host writes "1" to this bit to clear CEC Receive status interrupt

7.7 VIP Registers

7.7.1 Video IP Control, Status & Miscellaneous Registers

7.7.1.1 VBEMS_COM_TEST (VBEMS_COM_TEST:0x4000)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[10:3]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[2:0]			com_ipnr_sel	Reserved[3:0]			
Type	RO			R/W_1st	RO			
Default	0			0	0			
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[7:0]							com_mtx_sel
Type	RO							R/W_1st
Default	0x00							0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[2:0]			com_csf_sel	Reserved[2:0]			com_slv_sel

Type	RO			R/W_1st	RO			R/W_1st
Default	0			0	0			0

Table 7-37

Register Field	Bit	Default	Description
Reserved	[31:21]	0	
com_ipnr_sel	[20]	0	Bypass IPNR module (=1)
Reserved	[19:9]	0	
com_mtx_sel	[8]	0	Bypass MTX module (=1)
Reserved	[7:5]	0	
com_csf_sel	[4]	0	Bypass CSF module (=1)
Reserved	[3:1]	0	
com_slv_sel	[0]	0	Bypass SL module (=1)

7.7.1.2 vip_control (vip_control:0x6000)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	VipClkOff	Reserved						
Type	R/W	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved				pp_empty_err	vip_empty_err	pp_uflow	vip_oflow
Type	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						bitwidth[1:0]	
Type	RO	RO	RO	RO	RO	RO	R/W	
Default	0	0	0	0	0	0	0	1
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[6:0]					Autoscale_mode		vip_bypass
Type	RO					R/W		R/W
Default	0					0x0		1

Table 7-38

Register Field	Bit	Default	Description
VIPClkOff	[31]	0	VIP Clock Gate Off 0: VIP's clock is NOT gated off 1: VIP's clock can be gated off by the vip_bypass register bit vip_bypass = 1 means gated off vip_bypass = 0 means not gated off
Reserved	[30:18]	0	
pp_empty_err	[19]	0	PP FIFO Empty Error Set to 1 when PP FIFO is not empty when a new video frame is received. This bit will most probably always get set for first frame received after reset. So this bit should always be cleared by user after reset. Future assertions should be treated as real assertions.
vip_empty_err	[18]	0	VIP FIFO Empty Error

			Set to 1 when VIP FIFO is not empty when a new video frame is received. This bit will most probably always get set for first frame received after reset. So this bit should always be cleared by user after reset. Future assertions should be treated as real assertions.
pp_uflow	[17]	0	PP FIFO Underflow
vip_oflow	[16]	0	VIP FIFO Overflow
Reserved	[15:10]	0	
bitwidth	[9:8]	1	**Bit Width** IPNR 0: 8-bit video signal 1: 10-bit video signal (default) 2: 12-bit video signal
Reserved	[7:3]	0	Reserved
vcoefsel	[6:5]	0	Veritcal Coefficent Select Setting is valid only when autoscale mode is off. 0: from register 1: scale down to 480p 2: scale down 3: scale up
hcoefsel	[4:3]	0	Horizontal Coefficent Select Setting is valid only when autoscale mode is off. 0: from register 1: scale down to 480p 2: scale down 3: scale up
autoscale_mode	[2:1]	0	**Autoscale Mode** 0: Auto-scaling OFF 1: Output resolution is 480p 2: Output resolution is 720p 3: Output resolution is 1080p
vip_bypass	[0]	1	**VIP Bypass** 0: No bypass 1: Bypass VIP

7.7.1.3 VBEMS_CS_VLINE (VBEMS_CS_VLINE:0x5600)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				csa_r_vline			
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	1	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_r_vline							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-39 VBEMS_CS_VLINE

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
csa_r_vline	[11:0]	0	"Main data execution line counter value 0 origin"

7.7.1.4 VBEMS_CS_TAP_STATUS (VBEMS_CS_TAP_STATUS:0x5604)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	1	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							csa_r_tapdl_finx
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-40 VBEMS_CS_TAP_STATUS

Register Field	Bit	Default	Description
Reserved	[31:1]	0	
csa_r_tapdl_finx	[0]	0	Tap coefficient data transfer completed flag "0: Tap coefficient data transfer completed 1: Tap coefficient data transfer in progress * Update timing is startup signal falling"

7.7.1.5 VBEMS_CS_ERR (VBEMS_CS_ERR:0x5608)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	1	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							csa_r_err
Type	RO	RO	RO	RO	RO	RO	RO	R/W0C_S
Default	0	0	0	0	0	0	0	0

Table 7-41 VBEMS_CS_TAP_STATUS

Register Field	Bit	Default	Description
Reserved	[31:1]	0	
csa_r_err	[0]	0	Transfer completed flag 0: Ended when startup signal is input 1: Not ended when startup signal is input ∗ Update timing is startup signal rising

7.7.1.6 VIP_3D_CTRL (VIP_3D_CTRL:0x6530)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							top_bottom_3d
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	0	0

Table 7-42 VIP_3D_CTRL

Register Field	Bit	Default	Description
Reserved	[31:1]	0	
top_bottom_3d	[0]	0	Top and Bottom 3D 0 - disable, 1- enable

7.7.1.7 TOP_INPUT_PIXEL (TOP_INPUT_PIXEL:0x6534)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				top_input_pixel[27:24]			
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	top_input_pixel[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	top_input_pixel15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	top_input_pixel7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 7-43 TOP_INPUT_PIXEL

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
top_input_pixel	[27:16]	0	Top input pixel

7.7.1.8 TOP_OUTPUT_PIXEL (TOP_OUTPUT_PIXEL:0x6538)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				top_output_pixel[27:24]			
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	top_output_pixel[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	top_output_pixel[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	top_output_pixel[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 7-44 TOP_OUTPUT_PIXEL

Register Field	Bit	Default	Description
Reserved	[31:28]	0	

Register Field	Bit	Default	Description
top_output_pixel	[27:0]	0	Top output pixel

7.7.1.9 VIP_HAS (VIP_HAS:0x653C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved			vip_has_enable	Reserved			
Type	RO	RO	RO	R/W	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				vip_has			
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	vip_has							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 7-45 TOP_OUTPUT_PIXEL

Register Field	Bit	Default	Description
Reserved	[31:29]	0	
vip_has_enable	[28]	0	LCDCTRL Horizontal Active Space Enable 1: ON 0: OFF
Reserved	[27:12]	0	
vip_has	[11:0]	0	LCDCTRL Horizontal Active Space 0 = 1 pixel 1 = 2 pixels .... 1023 = 1024 pixels

7.7.2 De-Interlacer Registers

7.7.2.1 VBEMS_IP_FIELDID (VBEMS_IP_FIELDID:0x4080)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[30:23]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[22:15]							

Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[6:0]					Ip_FIELDSEL		ip_FIELDID
Type	RO					R/W_1st	R/W_1st	R/W_1st
Default	0					0	0	0

Table 7-46

Register Field	Bit	Default	Description
Reserved	[31:3]	0	
ip_FIELDSEL	[2:1]	0	Input signal field select 0: use ip_FIELDID below 1: use HDMIRX field index 2: use Inverted HDMIRX field index 3: Reserved
ip_FIELDID	[0]	0	Input signal field index 0: Bottom field 1: Top field

7.7.2.2 VBEMS_IP_MAIN_CNT (VBEMS_IP_MAIN_CNT:0x4084)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved		ip_NRON	ip_IPON	Reserved			
Type	RO		R/W_1st	R/W_1st	RO			
Default	0		0	0	0			
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved			ip_IPFMSEL	Reserved	ip_IPDLYMODE	ip_YIPMODE	ip_CIPMODE
Type	RO			R/W_1st	RO	R/W_1st	R/W_1st	R/W_1st
Default	0			0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved	ip_CSMPLTYPE[2:0]			Reserved[1:0]		ip_CFORMAT[1:0]	
Type	RO	R/W_1st			RO		R/W_1st	
Default	0	0			0		0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[2:0]			ip_SCANFORMAT	Reserved[3:0]			
Type	RO			R/W_1st	RO			
Default	0			0	0			

Table 7-47

Register Field	Bit	Default	Description
Reserved	[31:30]	0	
ip_NRON	[29]	0	**NR SW** 0: NR OFF

Register Field	Bit	Default	Description
			1: NR ON
ip_IPON	[28]	0	**IPSW** 0: IPC OFF 1: IPC ON
Reserved	[27:21]	0	
ip_IPFMSEL	[20]	0	**Frame delay signal selection for IP conversion** 0: Independent of for NR 1: Same as for NR
Reserved	[19]	0	
ip_IPDLYMODE	[18]	0	**IP conversion delay mode** 0: Normal mode 1: Low delay mode
ip_YIPMODE	[17]	0	**Y signal IP conversion mode** 0: Motion adaptation 1: Within field
ip_CIPMODE	[16]	0	**C signal IP conversion mode** 0: Motion adaptation 1: Within field
Reserved	[15]	0	
ip_CSMPLTYPE	[14:12]	0	**C signal sample type (when 4:2:0)** 0: type 0 to 5: type 5, 6-7: type 5
Reserved	[11:10]	0	
ip_CFORMAT	[9:8]	0	**Input signal color format** 0: 4:2:0 1: 4:2:2 2-3: 4:4:4
Reserved	[7:5]	0	
ip_SCANFORMAT	[4]	0	**Input signal scan format** 0: Progressive 1: Interlace
Reserved	[3:0]	0	

7.7.2.3 VBEMS_IP_SRC_WIDTH (VBEMS_IP_SRC_WIDTH:0x4088)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[18:11]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[10:3]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[2:0]			ip_IPNRWIDTH[12:8]				
Type	RO			R/W_1st				
Default	0			720				
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	ip_IPNRWIDTH[7:0]							
Type	R/W_1st							
Default	720							

Table 7-48

Register Field	Bit	Default	Description
Reserved	[31:13]	0	
ip_IPNRWIDTH	[12:0]	720	**Original image horizontal size** 2 to 4096 pixels (even numbered only) : During ipnr through mode 256 to 1920 pixels (even numbered only) : During ipnr operation

7.7.2.4 VBEMS_IP_SRC_HEIGHT (VBEMS_IP_SRC_HEIGHT:0x408C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved		ip_IPNRHEIGHT[13:8]					
Type	RO		R/W_1st					
Default	0		240					
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ip_IPNRHEIGHT[7:0]							
Type	R/W_1st							
Default	240							

Table 7-49

Register Field	Bit	Default	Description
Reserved	[31:14]	0	
ip_IPNRHEIGHT	[13:0]	240	**Original image vertical size** Set in Y value, during interlace is 1/2 during progressive 2 to 8192 lines (even numbered only) : During ipnr through mode 8 to 1200 lines (even numbered only) : During ipnr operation

7.7.2.5 VBEMS_IP_IP_SIP_MODE (VBEMS_IP_IP_SIP_MODE:0x416C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved						ip_ipsip_modsel	
Type	RO						R/W_1st	
Default	0						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved			ip_ipsip_flphinv	Reserved			ip_ipsip_off
Type	RO			R/W_1st	RO			R/W_1st
Default	0			0	0			0

Table 7-50

Register Field	Bit	Default	Description
Reserved	[31:10]	0	
ip_ipsip_modsel	[9:8]	0	**Direction judgment median filter mode** 0: 5tap, 1: 3tap, 2: OFF, 3: Reserved
Reserved	[7:5]	0	
ip_ipsip_flphinv	[4]	0	**SIP FLPH polarity** 0: Normal, 1: Inverted
Reserved	[3:1]	0	
ip_ipsip_off	[0]	0	**SIP motion mode** 0: ON, 1 : OFF (up-down sum)

7.7.2.6 VBEMS_IP_IP_SIP_EDGLEV (VBEMS_IP_IP_SIP_EDGLEV:0x4170)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							ip_ipsip_edglev[8]
Type	RO							R/W_1st
Default	0							256
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	ip_ipsip_edglev[7:0]							
Type	R/W_1st							
Default	256							

Table 7-51

Register Field	Bit	Default	Description
Reserved	[31:9]	0	
ip_ipsip_edglev	[8:0]	256	SIP edge inverted level

7.7.2.7 VBEMS_IP_IP_SIP_DLEV (VBEMS_IP_IP_SIP_DLEV:0x4174)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	ip_ipsip_mindsft[3:0]				Reserved	ip_ipsip_blkdlev[10:8]		
Type	R/W_1st				RO	R/W_1st		
Default	1				0	2047		
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	ip_ipsip_blkdlev[7:0]							
Type	R/W_1st							
Default	2047							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[5:0]						ip_ipsip_lindlev[9:8]	
Type	RO						R/W_1st	
Default	0						1023	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ip_ipsip_lindlev[7:0]							
Type	R/W_1st							
Default	1023							

Table 7-52

Register Field	Bit	Default	Description
ip_ipsip_mindsft	[31:28]	1	SIP judgment level shift
Reserved	[27]	0	
ip_ipsip_blkdlev	[26:16]	2047	SIP block differential judgment level
Reserved	[15:10]	0	
ip_ipsip_lindlev	[9:0]	1023	SIP block differential judgment level

7.7.2.8 VBEMS_IP_IP_SIP_IKC (VBEMS_IP_IP_SIP_IKC:0x4178)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[6:0]							ip_ipsip_lnedg
Type	RO							R/W_1st
Default	0							0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ip_ipsip_ikfor	Reserved[1:0]		ip_ipsip_ikflev[4:0]				
Type	R/W_1st	RO		R/W_1st				
Default	1	0		0				
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[2:0]			ip_ipsip_ikcore[4:0]				
Type	RO			R/W_1st				
Default	0			8				

Table 7-53

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
ip_ipsip_lnedg	[16]	0	Line edge detect judgment 1: ON, 0: OFF
ip_ipsip_ikfor	[15]	1	Forced fixed MIX 1: OFF, 0: ON
Reserved	[14:13]	0	
ip_ipsip_ikflev	[12:8]	0	Forced MIX level
Reserved	[7:5]	0	
ip_ipsip_ikcore	[4:0]	8	MIX level nonlinear coring

7.7.2.9 VBEMS_IP_IP_C_CNT (VBEMS_IP_IP_C_CNT:0x4180)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							ip_CDIRUDINV
Type	RO							R/W_1st
Default	0							0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved						ip_CMIP_SEL[1:0]	
Type	RO						R/W_1st	
Default	0						2	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							ip_CPAIOFF
Type	RO							R/W_1st
Default	0							0

Table 7-54

Register Field	Bit	Default	Description
Reserved	[31:25]	0	
ip_CDIRUDINV	[24]	0	**C direct line output selection** 0: Normal 1: Reverse
Reserved	[23:18]	0	
ip_CMIP_SEL	[17:16]	2	**Up-down interpolation method when C picture adaptation interpolation OFF** 00: 2 degree swing 01: Up 3: Down 1 10: Up 1: Down 1 11: Up 1: Down 3
Reserved	[15:1]	0	
ip_CPAIOFF	[0]	0	**C picture adaptation interpolation OFF** 0: Picture adaptation ON 1: Picture adaptation OFF

7.7.2.10 VBEMS_SR_MODE (VBEMS_SR_MODE:0x4380)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	sr_c_ofsh	sr_c_ofsv[2:0]			sr_cexp_mode[1:0]		sr_cinfmt[1:0]	
Type	R/W_1st	R/W_1st			R/W_1st		R/W_1st	
Default	0	0			0		0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[2:0]			sr_inmode	Reserved			
Type	RO			R/W_1st	RO			
Default	0			0	0			

Table 7-55

Register Field	Bit	Default	Description
Reserved	[31:16]	0	
sr_c_ofsh	[15]	0	**420, 422 C input horizontal offset** 0: 0 1: 0.5
sr_c_ofsv	[14:12]	0	**420 C input vertical offset** 0: 0 1: 0.25 2: 0.5 3: 0.75 4-7: 1.0
sr_cexp_mode	[11:10]	0	**C extension mode** 0: Normal, 1: Horizontal linear interpolation, 2: Vertical linear interpolation, 3: Horizontal and vertical linear interpolation
sr_cinfmt	[9:8]	0	**C input format** 0: 420, 1: 422, 2-3: 444
Reserved	[7:5]	0	
sr_inmode	[4]	0	**SRF input mode** 0: 2 line input, 1: 1 line input
Reserved	[3:0]	0	

7.7.2.11 VBEMS_SR_HVSZIN (VBEMS_SR_HVSZIN:0x4384)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved			sr_hszin[12:8]				
Type	RO			R/W_1st				
Default	0			720				
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	sr_hszin[7:0]							
Type	R/W_1st							
Default	720							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved		sr_vszin[13:8]					
Type	RO		R/W_1st					
Default	0		480					
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	sr_vszin[7:0]							
Type	R/W_1st							
Default	480							

Table 7-56

Register Field	Bit	Default	Description
Reserved	[31:29]	0	
sr_hszin	[28:16]	720	SRF input horizontal pixel number
Reserved	[15:14]	0	
sr_vszin	[13:0]	480	SRF input vertical line number

7.7.2.12 VBEMS_DE_SIZE (VBEMS_DE_SIZE:0x4484)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved				de_hsize[11:8]			
Type	RO				R/W_1st			
Default	0				1920			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	de_hsize[7:0]							
Type	R/W_1st							
Default	1920							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				de_vsize[11:8]			
Type	RO				R/W_1st			
Default	0				1080			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	de_vsize[7:0]							
Type	R/W_1st							
Default	1080							

Table 7-57

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
de_hsize	[27:16]	1920	Horizontal image size
Reserved	[15:12]	0	
de_vsize	[11:0]	1080	Vertical image size

7.7.3 Scaler Registers

7.7.3.1 VBEMS_CS_MODE (VBEMS_CS_MODE:0x5040)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[6:0]							csa_act

Type	RO							R/W_1st
Default	0							1
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[6:0]							Reserved(csa_hisact)
Type	RO							RO
Default	0							0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	Reserved(csa_inmode)[2:0]			Reserved[2:0]			Reserved(csa_filmode)
Type	RO	RO			RO			RO
Default	0	0			0			0

Table 7-58

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
csa_act	[16]	1	CSF module execution setting 0: Operation off 1: Operation on
Reserved	[15:9]	0	
Reserved(csa_hisact)	[8]	0	HIS output setting 0: Output off 1: Output on
Reserved	[7]	0	
Reserved(csa_inmode)	[6:4]	0	Input format setting 0:4:4:4(Y:Cb:Cr) 1port input 3:4:2:2(Y:Cb/Cr) YC independent 2port input 4:4:2:0(Y:Cb/Cr) 2port input Settings other than above not possible
Reserved	[3:1]	0	
Reserved(csa_filmode)	[0]	0	Filter mode setting 0: Horizontal multiscaling filter, Vertical scaling filter, Horizontal straight interpolation scaling filter (Horizontal multiscaling filter PHOS valid: Horizontal straight interpolation scaling filter PHOS" 0" fixed)

7.7.3.2 VBEMS_CS_YHVSIN (VBEMS_CS_YHVSIN:0x5044)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[2:0]			csa_yhszin[12:8]				
Type	RO			R/W_1st				
Default	0			0				
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	csa_yhszin[7:0]							
Type	R/W_1st							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[1:0]		csa_yvszin[13:8]					
Type	RO		R/W_1st					

Default	0		0					
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_yvszin[7:0]							
Type	R/W_1st							
Default	0							

Table 7-59

Register Field	Bit	Default	Description
Reserved	[31:29]	0	Input Y horizontal pixel number When com_csa_direct_in = 1, only, valid
csa_yhszin	[28:16]	0	
Reserved	[15:14]	0	Input Y line number When com_csa_direct_in = 1, only, valid
csa_yvszin	[13:0]	0	Input Y horizontal pixel number When com_csa_direct_in = 1, only, valid

7.7.3.3 VBEMS_CS_CHVSIN (VBEMS_CS_CHVSIN:0x5048)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[2:0]			csa_chszin[12:8]				
Type	RO			R/W_1st				
Default	0			0				
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	csa_chszin[7:0]							
Type	R/W_1st							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[1:0]		csa_cvszin[13:8]					
Type	RO		R/W_1st					
Default	0		0					
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_cvszin[7:0]							
Type	R/W_1st							
Default	0							

Table 7-60

Register Field	Bit	Default	Description
Reserved	[31:29]	0	
csa_chszin	[28:16]	0	Input C horizontal pixel number When com_csa_direct_in = 1, only, valid
Reserved	[15:14]	0	
csa_cvszin	[13:0]	0	com_csa_direct_in = 1

7.7.3.4 VBEMS_CS_HSZOUT (VBEMS_CS_HSZOUT:0x504C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24

Name	Reserved[4:0]					csa_hszout[10:8]		
Type	RO					R/W_1st		
Default	0					0		
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	csa_hszout[7:0]							
Type	R/W_1st							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				csa_vszout[11:8]			
Type	RO				R/W_1st			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_vszout[7:0]							
Type	R/W_1st							
Default	0							

Table 7-61

Register Field	Bit	Default	Description
Reserved	[31:27]	0	
csa_hszout	[26:16]	0	Output pixel number
Reserved	[15:12]	0	
csa_vszout	[11: 0]	0	Output line number

7.7.3.5 VBEMS_CS_YHFILMODE (VBEMS_CS_YHFILMODE:0x5050)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[4:0]					csa_ymhfil_hszout[10:8]		
Type	RO					R/W_1st		
Default	0					0		
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	csa_ymhfil_hszout[7:0]							
Type	R/W_1st							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[10:3]							
Type	RO							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[2:0]			csa_yhfil_thmode	Reserved	csa_yhfil_mode[2:0]		
Type	RO			R/W_1st	RO	R/W_1st		
Default	0			0	0	0		

Table 7-62

Register Field	Bit	Default	Description
Reserved	[31:27]	0	
csa_ymhfil_hszout	[26:16]	0	Horizontal multi-scaling filter output pixel number for Y

Register Field	Bit	Default	Description
			Shared with vertical filter input pixel number
Reserved	[15:5]	0	
csa_yhfil_thmode	[4]	0	Horizontal straight interpolation filter through tap setting for Y 0:off 1:on Through tap is 3tap interpolation
Reserved	[3]	0	
csa_yhfil_mode	[2:0]	0	Horizontal filter mode for Y 0:16 tap 16ovs 1:8 tap 32ovs 2:4 tap 64ovs 3:2 tap 128ovs 4:2 tap 256ovs 5:2 tap 512ovs 6:Nearest neighbor (2 degree swing) 7: setting is prohibited

7.7.3.6 VBEMS_CS_YHFILPSMODE (VBEMS_CS_YHFILPSMODE:0x5054)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[6:0]							csa_yhfil_psact
Type	RO							R/W_1st
Default	0							0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[2:0]			csa_yhfil_szin[12:8]				
Type	RO			R/W_1st				
Default	0			0				
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_yhfil_szin[7:0]							
Type	R/W_1st							
Default	0							

Table 7-63

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
csa_yhfil_psact	[16]	0	Filter horizontal pixel clipping valid for Y 0: No input horizontal pixel clipping 1: With input horizontal pixel clipping
Reserved	[15:13]	0	
csa_yhfil_szin	[12:0]	0	Horizontal filter processed horizontal pixel number for Y

7.7.3.7 VBEMS_CS_YMHFILBASE (VBEMS_CS_YMHFILBASE:0x505C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[9:2]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[1:0]		csa_ymhfil_base[18:13]					
Type	RO		R/W_1st					
Default	0		0					
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	csa_ymhfil_base[12:5]							
Type	R/W_1st							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_ymhfil_base[4:0]					Reserved[2:0]		
Type	R/W_1st					RO		
Default	0					0		

Table 7-64

Register Field	Bit	Default	Description
Reserved	[31:22]	0	
csa_ymhfil_base	[21:3]	0	Horizontal multi-scaling filter interval for Y 0x10000 integer area 6bit decimal area 13bit Setting range "0x200000 to 0x01000", 0x8 steps Even with horizontal filter OFF, 0x10000 setting required
Reserved	[2:0]	0	Bottom 3 bits of decimal area not used.

7.7.3.8 VBEMS_CS_YLHFILBASE (VBEMS_CS_YLHFILBASE:0x5060)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							csa_ylhfil_ovs
Type	RO							R/W_1st
Default	0							0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved		csa_ylhfil_base[18:13]					
Type	RO		R/W_1st					
Default	0		0x01					
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	csa_ylhfil_base[12:5]							
Type	R/W_1st							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_ylhfil_base[4:0]					Reserved		
Type	R/W_1st					RO		
Default	0					0		

Table 7-65

Register Field	Bit	Default	Description
Reserved	[31:25]	0	
csa_ylhfil_ovs	[24]	0	Horizontal straight interpolation scaling filter over sampling mode for Y 0: 256 over sampling 1: 512 over sampling
Reserved	[23:22]	0	
csa_ylhfil_base	[21:3]	0x02000	Horizontal straight interpolation scaling filter interval for Y 1x: 0x10000 integer area 6bit decimal area 13bit Setting range "0x200000 to 0x01000", 0x8 steps Even with horizontal filter OFF, 0x10000 setting required
Reserved	[2:0]	0	Bottom 3 bits of decimal area not used.

7.7.3.9 VBEMS_CS_CHFILMODE (VBEMS_CS_CHFILMODE:0x5070)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[4:0]					csa_cmhfil_hszout[10:8]		
Type	RO					R/W_1st		
Default	0					0		
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	csa_cmhfil_hszout[7:0]							
Type	R/W_1st							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[10:3]							
Type	RO							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	Reserved[2:0]			csa_chfil_thmode	Reserved	csa_chfil_mode[2:0]		
Type	RO			R/W_1st	RO	R/W_1st		
Default	0			0	0	0		

Table 7-66

Register Field	Bit	Default	Description
Reserved	[31:27]	0	
csa_cmhfil_hszout	[26:16]	0	Horizontal multi-scaling filter output pixel number for C Shared with vertical filter input pixel number
Reserved	[15:5]	0	
csa_chfil_thmode	[4]	0	Horizontal straight interpolation filter through tap setting for C 0:off 1:on Through tap is 3tap interpolation
Reserved	[3]	0	
csa_chfil_mode	[2:0]	0	Horizontal filter mode for C 0:16 tap 16ovs 1:8 tap 32ovs 2:4 tap 64ovs 3:2 tap 128ovs 4:2 tap 256ovs 5:2 tap 512ovs 6:Nearest neighbor (2 degree swing) 7: setting is prohibited

7.7.3.10 VBEMS_CS_CHFILPSMODE (VBEMS_CS_CHFILPSMODE:0x5074)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[6:0]							csa_chfil_psact
Type	RO							R/W_1st
Default	0							0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[2:0]			csa_chfil_szin[12:8]				
Type	RO			R/W_1st				
Default	0			0				
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_chfil_szin[7:0]							
Type	R/W_1st							
Default	0							

Table 7-67

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
csa_chfil_psact	[16]	0	Filter horizontal pixel clipping valid for C 0: No input horizontal pixel clipping 1: With input horizontal pixel clipping
Reserved	[15:13]	0	
csa_chfil_szin	[12:0]	0	Horizontal filter processed horizontal pixel number for C

7.7.3.11 VBEMS_CS_CPHOS (VBEMS_CS_CPHOS:0x5078)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[1:0]		csa_cphos[22:17]					
Type	RO		R/W_1st					
Default	0		0					
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	csa_cphos[16:9]							
Type	R/W_1st							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	csa_cphos[8:1]							
Type	R/W_1st							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_cphos	Reserved[6:0]						
Type	R/W_1st	RO						
Default	0	0						

Table 7-68

Register Field	Bit	Default	Description
Reserved	[31:30]	0	
csa_cphos	[29:7]	0	Horizontal clipping start position for C [29:16]: Pixel clipping position [15:7]: Pixel internal clipping position
Reserved	[6:0]	0	Bottom 7 bits of decimal area not used.

7.7.3.12 VBEMS_CS_CMHFILBASE (VBEMS_CS_CMHFILBASE:0x507C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[9:2]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[1:0]		csa_cmhfil_base[18:13]					
Type	RO		R/W_1st					
Default	0		0					
Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	csa_cmhfil_base[12:5]							
Type	R/W_1st							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_cmhfil_base[4:0]					Reserved[2:0]		
Type	R/W_1st					RO		
Default	0					0		

Table 7-69

Register Field	Bit	Default	Description
Reserved	[31:22]	0	
csa_cmhfil_base	[21:3]	0	Horizontal multi-scaling filter interval for C 0x10000 integer area 6bit decimal area 13bit Setting range "0x200000 to 0x01000", 0x8 steps Even with horizontal filter OFF, 0x10000 setting required
Reserved	[2:0]	0	Bottom 3 bits of decimal area not used.

7.7.3.13 VBEMS_CS_CLHFILBASE (VBEMS_CS_CLHFILBASE:0x5080)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							csa_clhfil_ovs
Type	RO							R/W_1st
Default	0							0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved		csa_clhfil_base[18:13]					
Type	RO		R/W_1st					
Default	0		0x01					
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	csa_clhfil_base[12:5]							
Type	R/W_1st							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_clhfil_base[4:0]					Reserved		
Type	R/W_1st					RO		
Default	0					0		

Table 7-70

Register Field	Bit	Default	Description
Reserved	[31:25]	0	
csa_clhfil_ovs	[24]	0	Horizontal straight interpolation scaling filter over sampling mode for C 0: 256 over sampling 1: 512 over sampling
Reserved	[23:22]	0	
csa_clhfil_base	[21:3]	0x2000	Horizontal straight interpolation scaling filter interval for C 1x: 0x10000 integer area 8bit decimal area 13bit Setting range "0x200000 to 0x01000", 0x8 steps Even with horizontal filter OFF, 0x10000 setting required

Register Field	Bit	Default	Description
Reserved	[2:0]	0	Bottom 3 bits of decimal area not used.

7.7.3.14 VBEMS_CS_YVFILMODE (VBEMS_CS_YVFILMODE:0x5090)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[26:19]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[18:11]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[10:3]							
Type	RO							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[2:0]			csa_yvfil_thmode	Reserved	csa_yvfil_mode[2:0]		
Type	RO			R/W_1st	RO	R/W_1st		
Default	0			0	0	0		

Table 7-71

Register Field	Bit	Default	Description
Reserved	[31:5]	0	
csa_yvfil_thmode	[4]	0	Vertical straight interpolation filter through tap setting for Y 0:off 1:on Through tap is 3tap interpolation
Reserved	[3]	0	
csa_yvfil_mode	[2:0]	0	Vertical filter mode for Y 0:8 tap 32ovs 1:4 tap 64ovs 2:2 tap 128ovs 3:2 tap 256ovs 4:2 tap 512ovs 5:Nearest neighbor (2 degree swing) 6, 7 setting is prohibited

7.7.3.15 VBEMS_CS_YVFILPSMODE (VBEMS_CS_YVFILPSMODE:0x5094)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[14:7]							
Type	RO							
Default	0							

Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[6:0]							csa_yvfil_psact
Type	RO							R/W_1st
Default	0							0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[1:0]		csa_yvfil_szin[13:8]					
Type	RO		R/W_1st					
Default	0		0					
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_yvfil_szin[7:0]							
Type	R/W_1st							
Default	0							

Table 7-72

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
csa_yvfil_psact	[16]	0	Filter vertical line clipping valid for Y 0: No input vertical line clipping 1: With input vertical line clipping
Reserved	[15:14]	0	
csa_yvfil_szin	[13:0]	0	Vertical filter processed line number for Y (min 1 line, max 8192 lines)

7.7.3.16 VBEMS_CS_YPVOS_TOP (VBEMS_CS_YPVOS_TOP:0x5098)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved	csa_ypvos_top_top[23:17]						
Type	RO	R/W_1st						
Default	0	0x00						
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	csa_ypvos_top[16:9]							
Type	R/W_1st							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	csa_ypvos_top[8:1]							
Type	R/W_1st							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_ypvos_top	Reserved						
Type	R/W_1st	RO						
Default	0	0x00						

Table 7-73

Register Field	Bit	Default	Description
Reserved	[31]	0	
csa_ypvos_top	[30:7]	0	Vertical clipping start position for Y

Register Field	Bit	Default	Description
			[30:16]: Pixel clipping position [15:7]: Pixel internal clipping position
Reserved	[6:0]	0	Bottom 7 bits of decimal area not used.

7.7.3.17 VBEMS_CS_YVFILBASE (VBEMS_CS_YVFILBASE:0x509C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[9:2]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[1:0]		csa_yvfil_base[18:13]					
Type	RO		R/W_1st					
Default	0		0					
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	csa_yvfil_base[12:5]							
Type	R/W_1st							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_yvfil_base[4:0]					Reserved[2:0]		
Type	R/W_1st					RO		
Default	0					0		

Table 7-74

Register Field	Bit	Default	Description
Reserved	[31:22]	0	
csa_yvfil_base	[21:3]	0	Vertical filter interval for Y 0x10000 integer area 6bit decimal area 16bit Setting range "0x200000 to 0x01000", 0x8 steps Even with vertical filter OFF, 0x10000 setting required
Reserved	[2:0]	0	Bottom 3 bits of decimal area not used.

7.7.3.18 VBEMS_CS_CVFILMODE (VBEMS_CS_CVFILMODE:0x50A0)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[26:19]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[18:11]							
Type	RO							

Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[10:3]							
Type	RO							
Default	0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[2:0]			csa_cvfil_thmode	Reserved	csa_cvfil_mode[2:0]		
Type	RO			R/W_1st	RO	R/W_1st		
Default	0			0	0	0		

Table 7-75

Register Field	Bit	Default	Description
Reserved	[31:5]	0	
csa_cvfil_thmode	[4]	0	Vertical straight interpolation filter through tap setting for C 0:off 1:on Through tap is 3tap interpolation
Reserved	[3]	0	
csa_cvfil_mode	[2:0]	0	Vertical filter mode for C 0:8 tap 32ovs 1:4 tap 64ovs 2:2 tap 128ovs 3:2 tap 256ovs 4:2 tap 512ovs 5:Nearest neighbor (2 degree swing) 6, 7 setting is prohibited

7.7.3.19 VBEMS_CS_CVFILPSMODE (VBEMS_CS_CVFILPSMODE:0x50A4)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[6:0]							csa_cvfil_psact
Type	RO							R/W_1st
Default	0							0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[1:0]		csa_cvfil_szin[13:8]					
Type	RO		R/W_1st					
Default	0		0					
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	csa_cvfil_szin[7:0]							
Type	R/W_1st							
Default	0							

Table 7-76

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
csa_cvfil_psact	[16]	0	Filter vertical line clipping valid for C 0: No input vertical line clipping 1: With input vertical line clipping
Reserved	[15:14]	0	
csa_cvfil_szin	[13:0]	0	Vertical filter processed line number for C (min 1 line, max 8192 lines)

7.7.3.20 VBEMS_CS_CPVOS_TOP (VBEMS_CS_CPVOS_TOP:0x50A8)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved	csa_cpvos_top[23:17]						
Type	RO	R/W_1st						
Default	0	0x00						
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	csa_cpvos_top[16:9]							
Type	R/W_1st							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	csa_cpvos_top[8:1]							
Type	R/W_1st							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_cpvos_top	Reserved						
Type	R/W_1st	RO						
Default	0	0x00						

Table 7-77

Register Field	Bit	Default	Description
Reserved	[31]	0	
csa_cpvos_top	[30:7]	0	Vertical clipping start position for C [30:16]: Pixel clipping position [15:7]: Pixel internal clipping position
Reserved	[6:0]	0	Bottom 7 bits of decimal area not used.

7.7.3.21 VBEMS_CS_CVFILBASE (VBEMS_CS_CVFILBASE:0x50AC)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[9:2]							
Type	RO							
Default	0							

Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[1:0]		csa_cvfil_base[18:13]					
Type	RO		R/W_1st					
Default	0		0					
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	csa_cvfil_base[12:5]							
Type	R/W_1st							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_cvfil_base[4:0]					Reserved[2:0]		
Type	R/W_1st					RO		
Default	0					0		

Table 7-78

Register Field	Bit	Default	Description
Reserved	[31:22]	0	
csa_cvfil_base	[21:3]	0	Vertical filter interval for C 0x10000 integer area 6bit decimal area 16bit Setting range "0x200000 to 0x01000", 0x8 steps Even with vertical filter OFF, 0x10000 setting required
Reserved	[2:0]	0	Bottom 3 bits of decimal area not used.

7.7.3.22 VBEMS_CS_YPVOS_BOTTOM (VBEMS_CS_YPVOS_BOTTOM:0x50B0)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved	csa_ypvos_bottom						
Type	RO	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	csa_ypvos_bottom							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	csa_ypvos_bottom							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_ypvos_bottom	Reserved						
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-79 VBEMS_CS_YPVOS_BOTTOM

Register Field	Bit	Default	Description
Reserved	[31]	0	
csa_cvfil_base	[30:7]	0	Vertical clipping start position for Y [30:16]: Pixel clipping position

Register Field	Bit	Default	Description
			[15:7]: Pixel internal clipping position
Reserved	[6:0]	0	Bottom 7 bits of decimal area not used.

7.7.3.23 VBEMS_CS_CPVOS_BOTTOM (VBEMS_CS_CPVOS_BOTTOM:0x50B4)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved	csa_cpvos_bottom						
Type	RO	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name								
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name								
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	csa_cpvos_bottom	Reserved						
Type	R/W_1st	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 7-80 VBEMS_CS_CPVOS_BOTTOM

Register Field	Bit	Default	Description
Reserved	[31]	0	
mtb_enable	[30:7]	0	Vertical clipping start position for C [30:16]: Pixel clipping position [15:7]: Pixel internal clipping position
Reserved	[6:0]	0	Bottom 7 bits of decimal area not used.

7.7.3.24 VBEMS_CS_PVOS_SELECT (VBEMS_CS_PVOS_SELECT:0x50B8)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						csa_pvos_select	
Type	RO	RO	RO	RO	RO	RO	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-81 VBEMS_CS_PVOS_SELECT

Register Field	Bit	Default	Description
Reserved	[31:2]	0	
csa_pvos_select	[1:0]	0	Vertical clipping start position select 0: TOP/BOTTOM 1: BoTTOM/TOP 2: TOP 3: BOTTOM

7.7.4 YCbCr to RGB Registers

7.7.4.1 VBEMS_MTB_ENABLE (VBEMS_MTB_ENABLE:0x5204)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							mtb_enable
Type	RO	RO	RO	RO	RO	RO	RO	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-82 VBEMS_MTB_ENABLE

Register Field	Bit	Default	Description
Reserved	[31:1]	0	
mtb_enable	[0]	0	Color space conversion matrix circuit Enable 0:Disable 1:Enable

7.7.4.2 VBEMS_MTB_Y_OFFSET (VBEMS_MTB_Y_OFFSET:0x5208)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							mtb_y_in_off[16:16]
Type	RO	RO	RO	RO	RO	RO	RO	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	mtb_y_in_off[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mtb_y_in_off[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-83 VBEMS_MTB_Y_OFFSET

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
mtb_y_in_off	[16:0]	0	VIDEO plane Input offset coefficient Y Set with 2 complements (-65536 to 65535)

7.7.4.3 VBEMS_MTB_G1 (VBEMS_MTB_G1:0x520C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	mtb_y_g_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	1	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mtb_y_g_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-84 VBEMS_MTB_G1

Register Field	Bit	Default	Description
Reserved	[31:16]	0	
mtb_y_g_coef	[15:0]	4096	VIDEO plane Conversion matrix coefficient Y→G Set with 2 complements (-32768 to 32767) 4096=1.0

7.7.4.4 VBEMS_MTB_G2 (VBEMS_MTB_G2:0x5210)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	mtb_cb_g_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	mtb_cb_g_coef[7:0]							

Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	mtb_cr_g_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mtb_cr_g_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-85 VBEMS_MTB_G2

Register Field	Bit	Default	Description
mtb_cb_g_coef	[31:16]	0	VIDEO plane Conversion matrix coefficient Cb→G Set with 2 complements (-32768 to 32767) 4096=1.0
mtb_cr_g_coef	[15:0]	0	VIDEO plane Conversion matrix coefficient Cr→G Set with 2 complements (-32768 to 32767) 4096=1.0

7.7.4.5 VBEMS_MTB_G_OFFSET (VBEMS_MTB_G_OFFSET:0x5214)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							mtb_g_out_off[16:16]
Type	RO	RO	RO	RO	RO	RO	RO	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	mtb_g_out_off[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	1	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mtb_g_out_off[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-86 VBEMS_MTB_G_OFFSET

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
mtb_g_out_off	[16:0]	4096	VIDEO plane Output offset coefficient G Set with 2 complements (-65536 to 65535)

7.7.4.6 VBEMS_MTB_CB_OFFSET (VBEMS_MTB_CB_OFFSET:0x5218)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[6:0]							mtb_cb_in_off[16:16]
Type	RO	RO	RO	RO	RO	RO	RO	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	mtb_cb_in_off[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	mtb_cb_in_off[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-87 VBEMS_MTB_CB_OFFSET

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
mtb_cb_in_off	[16:0]	0	VIDEO plane Input offset coefficient Cb Set with 2 complements (-65536 to 65535)

7.7.4.7 VBEMS_MTB_B1 (VBEMS_MTB_B1:0x521C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	mtb_y_b_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	mtb_y_b_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-88 VBEMS_MTB_B1

Register Field	Bit	Default	Description

Register Field	Bit	Default	Description
Reserved	[31:16]	0	
mtb_y_b_coef	[15:0]	0	VIDEO plane Conversion matrix coefficient Y→B Set with 2 complements (-32768 to 32767) 4096=1.0

7.7.4.8 VBEMS_MTB_B2 (VBEMS_MTB_B2:0x5220)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	mtb_cb_b_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	1	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	mtb_cb_b_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	mtb_cr_b_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	mtb_cr_b_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-89 VBEMS_MTB_B2

Register Field	Bit	Default	Description
mtb_cb_b_coef	[31:16]	4096	VIDEO plane Conversion matrix coefficient Cb→B Set with 2 complements (-32768 to 32767) 4096=1.0
mtb_cr_b_coef	[15:0]	0	VIDEO plane Conversion matrix coefficient Cr→B Set with 2 complements (-32768 to 32767) 4096=1.0

7.7.4.9 VBEMS_MTB_B_OFFSET (VBEMS_MTB_B_OFFSET:0x5224)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							mtb_b_out_off[16:16]
Type	RO	RO	RO	RO	RO	RO	RO	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	mtb_b_out_off[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	1	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	mtb_b_out_off[7:0]							

Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-90 VBEMS_MTB_B_OFFSET

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
mtb_b_out_off	[16:0]	32768	VIDEO plane Output offset coefficient B Set with 2 complements (-65536 to 65535)

7.7.4.10 VBEMS_MTB_CR_OFFSET (VBEMS_MTB_CR_OFFSET:0x5228)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							mtb_cr_in_off[16:16]
Type	RO	RO	RO	RO	RO	RO	RO	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	mtb_cr_in_off[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	mtb_cr_in_off[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-91 VBEMS_MTB_CR_OFFSET

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
mtb_cr_in_off	[16:0]	0	VIDEO plane Input offset coefficient Cr Set with 2 complements (-65536 to 65535)

7.7.4.11 VBEMS_MTB_R1 (VBEMS_MTB_R1:0x522C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	mtb_y_r_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mtb_y_r_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-92 VBEMS_MTB_R1

Register Field	Bit	Default	Description
Reserved	[31:16]	0	
mtb_y_r_coef	[15:0]	0	VIDEO plane Conversion matrix coefficient Y→R Set with 2 complements (-32768 to 32767) 4096=1.0

7.7.4.12 VBEMS_MTB_R2 (VBEMS_MTB_R2:0x5230)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	mtb_cb_r_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	mtb_cb_r_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	mtb_cr_r_coef[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	1	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mtb_cr_r_coef[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-93 VBEMS_MTB_R2

Register Field	Bit	Default	Description
mtb_cb_r_coef	[31:16]	0	VIDEO plane Conversion matrix coefficient Cb→R Set with 2 complements (-32768 to 32767) 4096=1.0
mtb_cr_r_coef	[15:0]	4096	VIDEO plane Conversion matrix coefficient Cr→R Set with 2 complements (-32768 to 32767) 4096=1.0

7.7.4.13 VBEMS_MTB_R_OFFSET (VBEMS_MTB_R_OFFSET:0x5234)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO

Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[6:0]							mtb_r_out_off[16:16]
Type	RO	RO	RO	RO	RO	RO	RO	R/W_1st
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	mtb_r_out_off[15:8]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	1	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mtb_r_out_off[7:0]							
Type	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st	R/W_1st
Default	0	0	0	0	0	0	0	0

Table 7-94 VBEMS_MTB_R_OFFSET

Register Field	Bit	Default	Description
Reserved	[31:17]	0	
mtb_r_out_off	[16:0]	32768	VIDEO plane Output offset coefficient R Set with 2 complements (-65536 to 65535)

7.7.5 Scaler (Horizontal – HSF) Registers

7.7.5.1 VBEMD_HSF_FILTER (VBEMD_HSF_FILTER:0x5920)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[17:10]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[9:2]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[1:0]		sl_ytap_sel[1:0]		Reserved[1:0]		sl_ctap_sel[1:0]	
Type	RO		R/W_1st		RO		R/W_1st	
Default	0		0		0		0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[1:0]		sl_tap_mode[1:0]		Reserved[2:0]			sl_filon
Type	RO		R/W_1st		RO			R/W_1st
Default	0		0		0			0

Table 7-95

Register Field	Bit	Default	Description
Reserved	[31:14]	0	
sl_ytap_sel	[13:12]	0	Y tap coefficient selection sl_tap_mode=0 (linear interpolation) 0: Center tap is 3tap interpolation 1: Center tap is through sl_tap_mode=1(16x oversampling)

Register Field	Bit	Default	Description
			At 0 to 3, select 4 types of coefficients. sl_tap_mode=2(128x oversampling) At 0 to 3, select 4 types of coefficients. sl_tap_mode=3 reserved
Reserved	[11:10]	0	
sl_ctap_sel	[9:8]	0	C tap coefficient selection sl_tap_mode=0 (linear interpolation) 0: Center tap is 3tap interpolation 1: Center tap is through sl_tap_mode=1(16x oversampling) At 0 to 3, select 4 types of coefficients. sl_tap_mode=2(128x oversampling) At 0 to 3, select 4 types of coefficients. sl_tap_mode=3 reserved
Reserved	[7:6]	0	
sl_tap_mode	[5:4]	0	tap mode selection 0: Linear interpolation 1: 12tap16 oversampling 2: 12tap128 oversampling 3: reserved
Reserved	[3:1]	0	
sl_filon	[0]	0	YC filter ON/OFF 0: filter_off 1: filter_on

7.7.5.2 VBEMD_HSF_HSZIN (VBEMD_HSF_HSZIN:0x5924)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[20:13]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[12:5]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[4:0]					sl_hszin[10:8]		
Type	RO					R/W_1st		
Default	0					1920		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	sl_hszin[7:0]							
Type	R/W_1st							
Default	1920							

Table 7-96

Register Field	Bit	Default	Description
Reserved	[31:11]	0	

Register Field	Bit	Default	Description
sl_hszin	[10:0]	1920	Input horizontal pixel number (maximum 1920)

7.7.5.3 VBEMD_HSF_HSZOUT (VBEMD_HSF_HSZOUT:0x5928)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[19:12]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[11:4]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				sl_hszout[11:8]			
Type	RO				R/W_1st			
Default	0				1920			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	sl_hszout[7:0]							
Type	R/W_1st							
Default	1920							

Table 7-97

Register Field	Bit	Default	Description
Reserved	[31:12]	0	
sl_hszout	[11: 0]	1920	Input horizontal pixel number (maximum 1920)

7.7.5.4 VBEMD_HSF_HFILBASE (VBEMD_HSF_HFILBASE:0x592C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[7:0]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	sl_hfilbase[23:16]							
Type	R/W_1st							
Default	65536							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	sl_hfilbase[15:8]							
Type	R/W_1st							
Default	65536							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	sl_hfilbase[7:0]							
Type	R/W_1st							
Default	65536							

Table 7-98

Register Field	Bit	Default	Description
Reserved	[31:24]	0	
sl_hfilbase	[23:0]	65536	Horizontal filter interval 1x: 0x10000 integer 8bit digital 16bit "Digital bottom 3bit not used. Even when horizontal filter OFF, 0x10000 setting is required" Corresponding magnification is 1x to 6x , 0x01_0000 to 0x0x00_1000

7.7.5.5 VBEMD_HSF_HINIT (VBEMD_HSF_HINIT:0x5958)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[10:3]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[2:0]			Reserved(sl_hinit)[20:16]				
Type	RO			RO				
Default	0			1817612				
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved(sl_hinit)[15:8]							
Type	RO							
Default	1817612							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved(sl_hinit)[7:0]							
Type	RO							
Default	1817612							

Table 7-99

Register Field	Bit	Default	Description
Reserved	[31:21]	0	
Reserved(sl_hinit)	[20:0]	1817612	Super Live Horizontal bias initial value. S+20

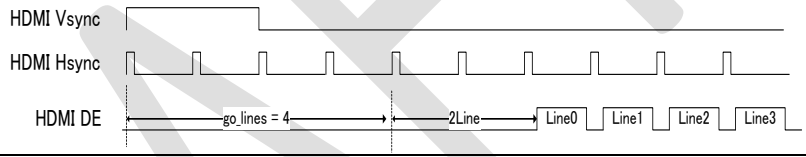
7.7.6 LCD Control Registers

7.7.6.1 go_lines (go_lines:0x6004)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[23:16]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[15:8]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**

Name	lcdc_1xclk_sel	Reserved[7:0]						
Type	R/W	RO						
Default	0	0						
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	go_lines[7:0]							
Type	R/W							
Default	0							

Table 7-100

Register Field	Bit	Default	Description
Reserved	[31:16]	0	Reserved
Reserved	[15]	0	**LCD Controller Clock Select** 0: 2 x CSI-2 Clock (Default) 1: 1 x CSI-2 Clock
Reserved	[14:8]	0	Reserved
go_lines	[7:0]	0	**Go Lines** Number of lines from VSYNC to the first active video line minus 1. See example below where go_lines should be set to 4. 

7.7.6.2 vd_delay (vd_delay:0x6008)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	vd_delay[31:24]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	vd_delay[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	vd_delay[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vd_delay[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

Table 7-101 vd_delay

Register Field	Bit	Default	Description

vd_delay	[31:0]	0x1	**VD Delay** Number of 250MHz clock cycles to delay VSYNC by to the LCDCTRL. Note that 0 is illegal.

7.7.6.3 vip_vsw (vip_vsw:0x600C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[20:13]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[12:5]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[4:0]					vip_vsw[10:8]		
Type	RO					R/W		
Default	0					0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vip_vsw[7:0]							
Type	R/W							
Default	0							

Table 7-102

Register Field	Bit	Default	Description
Reserved	[31:11]	0	
vip_vsw	[10:0]	0	Vsync Width register 0 = 1 line 1 = 2 lines . . . 2047 = 2048 lines

7.7.6.4 vip_vbp (vip_vbp:0x6010)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[20:13]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[12:5]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[4:0]					vip_vbp[10:8]		
Type	RO					R/W		

Default	0					0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vip_vbp[7:0]							
Type	R/W							
Default	0							

Table 7-103

Register Field	Bit	Default	Description
Reserved	[31:11]	0	
vip_vbp	[10:0]	0	Vertical Back Porch register 0 = 1 line 1 = 2 lines . . . 2047 = 2048 lines

7.7.6.5 vip_val (vip_vact:0x6014)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved				vip_vact[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vip_vactl[7:0]							
Type	R/W							
Default	0							

Table 7-104

Register Field	Bit	Default	Description
Reserved	[31:12]	0	
vip_val	[11:0]	0	Vertical Active Line register 0 = 1 line 1 = 2 lines . . . 4095 = 4096 lines

7.7.6.6 vip_vfp (vip_vfp:0x6018)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[20:13]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[12:5]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[4:0]					vip_vfp[10:8]		
Type	RO					R/W		
Default	0					0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	vip_vfp[7:0]							
Type	R/W							
Default	0							

Table 7-105

Register Field	Bit	Default	Description
Reserved	[31:11]	0	
vip_vfp	[10:0]	0	Vertical Front Porch register 0 = 1 line 1 = 2 lines . . . 2047 = 2048 lines

7.7.6.7 vip_hsw (vip_hsw:0x601C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[19:12]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[11:4]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				vip_hsw[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	vip_hsw[7:0]							

Type	R/W							
Default	0							

Table 7-106

Register Field	Bit	Default	Description
Reserved	[31:12]	0	
vip_hsw	[11:0]	0	Horizontal Sync Width register 0 = 1 eff_pixel 1 = 2 eff_pixels . . . 4095 = eff_4096 pixels Where, • eff_pixel = pixels * (eff_CSI-2_clk/(pclk*bpp/3)) • pclk = Required output resolution Pixel Clock • eff_CSI-2_clk = CSI-2_byte_clk * (# of CSI-2 lanes) • bpp = bits per pixel

7.7.6.8 vip_hbp (vip_hbp:0x6020)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[19:12]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[11:4]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				vip_hbp[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vip_hbp[7:0]							
Type	R/W							
Default	0							

Table 7-107

Register Field	Bit	Default	Description
Reserved	[31:12]	0	
vip_hbp	[11:0]	0	Horizontal Back Porch register 0 = 1 eff_pixel

			1 = 2 eff_pixels . . . 4095 = 4096 eff_pixels Where, • eff_pixel = pixels * (eff_CSI-2_clk/(pclk*bpp/3)) • pclk = Required output resolution Pixel Clock • eff_CSI-2_clk = CSI-2_byte_clk * (# of CSI-2 lanes) • bpp = bits per pixel

7.7.6.9 vip_hap (vip_hact:0x6024)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[19:12]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[11:4]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				vip_hact[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vip_hact[7:0]							
Type	R/W							
Default	0							

Table 7-108

Register Field	Bit	Default	Description
Reserved	[31:12]	0	
vip_hact	[11:0]	0	Horizontal Active Pixel register 0 = 1 pixel 1 = 2 pixels . . . 4095 = 4096 pixels

7.7.6.10 vip_hfp (vip_hfp:0x6028)

Bit	B31	B30	B29	B28	B27	B26	B25	B24

Name	Reserved[19:12]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[11:4]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				vip_hfp[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vip_hfp[7:0]							
Type	R/W							
Default	0							

Table 7-109

Register Field	Bit	Default	Description
Reserved	[31:12]	0	
vip_hfp	[11:0]	0	Horizontal Front Porch register 0 = 1 res_pixel 1 = 2 res_pixels . . . 4095 = 4096 res_pixels Where, • res_pixel = (hfp+hap) * (eff_CSI-2_clk/(pclk*bpp/3)) – hap • hap = Number of active pixels per line in output resolution • hfp = Horizontal front porch required for output resolution • pclk = Required output resolution Pixel Clock • eff_CSI-2_clk = CSI-2_byte_clk * (# of CSI-2 lanes) • bpp = bits per pixel

7.7.6.11 vip_vas (vip_vas:0x602C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved			vip_vas_enable	vip_vas_data[11:8]			
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	vip_vas_data[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved					vip_vas[10:8]		
Type	RO	RO	RO	RO	RO	R/W	R/W	R/W

Default	0	0	0	0	0	0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	vip_vas[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 7-110 vip_vas

Register Field	Bit	Default	Description
Reserved	[31:29]	0	
vip_vas_enable	[28]	0	Enable use of the vertical active space
vip_vas_data	[27:16]	0	Active space data
Reserved	[15:11]	0	
vip_vas	[10:0]	0	Vertical Active Space register 0 = 1 line 1 = 2 lines . . . 2047 = 2048 lines

7.7.7 Scaler (additional) Registers

7.7.7.1 cs_vdMYH (cs_vdMYH:0x6030)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[22:15]							
Type	RO							
Default	0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[6:0]							cs_vdactMYH_in
Type	RO							R/W
Default	0							1
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved[2:0]			cs_vdtidMYH_in[4:0]				
Type	RO			R/W				
Default	0			0				

Table 7-111

Register Field	Bit	Default	Description
Reserved	[31:9]	0	
cs_vdactMYH_in	[8]	1	
Reserved	[7:5]	0	
cs_vdtidMYH_in	[4:0]	0	

7.7.7.2 cs_vdMYV (cs_vdMYV:0x6034)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[22:15]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[6:0]							cs_vdactMYV_in
Type	RO							R/W
Default	0							1
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[2:0]			cs_vdtidMYV_in[4:0]				
Type	RO			R/W				
Default	0			1				

Table 7-112

Register Field	Bit	Default	Description
Reserved	[31:9]	0	
cs_vdactMYV_in	[8]	1	
Reserved	[7:5]	0	
cs_vdtidMYV_in	[4:0]	1	

7.7.7.3 cs_vdMCH (cs_vdMCH:0x6038)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[22:15]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[6:0]							cs_vdactMCH_in
Type	RO							R/W
Default	0							1
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[2:0]			cs_vdtidMCH_in[4:0]				
Type	RO			R/W				
Default	0			2				

Table 7-113

Register Field	Bit	Default	Description
Reserved	[31:9]	0	
cs_vdactMCH_in	[8]	1	
Reserved	[7:5]	0	
cs_vdtidMCH_in	[4:0]	2	

7.7.7.4 cs_vdMCV (cs_vdMCV:0x603C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[22:15]							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[14:7]							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[6:0]							cs_vdactMCV_in
Type	RO							R/W
Default	0							1
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[2:0]			cs_vdtidMCV_in[4:0]				
Type	RO			R/W				
Default	0			3				

Table 7-114

Register Field	Bit	Default	Description
Reserved	[31:9]	0	
cs_vdactMCV_in	[8]	1	
Reserved	[7:5]	0	
cs_vdtidMCV_in	[4:0]	3	

7.7.8 Scaler Coefficients

7.7.8.1 YH0_1 (YH0_1:0x6100)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yhcoef0[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	yhcoef0[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved[3:0]				yhcoef1[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	yhcoef1[7:0]							
Type	R/W							
Default	0							

Table 7-115

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yhcoef0	[27:16]	0	
Reserved	[15:12]	0	
yhcoef1	[11:0]	0	

7.7.8.2 YH2_3 (YH2_3:0x6104)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yhcoef2[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	yhcoef2[7:0]							
Type	R/W							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				yhcoef3[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	yhcoef3[7:0]							
Type	R/W							
Default	0							

Table 7-116

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yhcoef2	[27:16]	0	
Reserved	[15:12]	0	
yhcoef3	[11:0]	0	

7.7.8.3 YHm_n (m_n = 4_5..122_123) (YHm_n:0x6108 – 0x61F4)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yhcoef m[11:8]			
Type	RO				R/W			

Default	0				0			
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	yhcoef m[7:0]							
Type	R/W							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				yhcoef n[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	yhcoef n[7:0]							
Type	R/W							
Default	0							

Table 7-117

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yhcoef m	[27:16]	0	
Reserved	[15:12]	0	
yhcoef n	[11:0]	0	

7.7.8.4 YH124_125 (YH124_125:0x61F8)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yhcoef124[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	yhcoef124[7:0]							
Type	R/W							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				yhcoef125[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	yhcoef125[7:0]							
Type	R/W							
Default	0							

Table 7-118

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yhcoef124	[27:16]	0	
Reserved	[15:12]	0	
yhcoef125	[11:0]	0	

7.7.8.5 YH126_127 (YH126_127:0x61FC)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yhcoef126[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	yhcoef126[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				yhcoef127[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	yhcoef127[7:0]							
Type	R/W							
Default	0							

Table 7-119

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yhcoef126	[27:16]	0	
Reserved	[15:12]	0	
yhcoef127	[11:0]	0	

7.7.8.6 YV0_1 (YV0_1:0x6200)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yvcoef0[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	yvcoef0[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				yvcoef1[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	yvcoef1[7:0]							
Type	R/W							
Default	0							

Table 7-120

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yvcoef0	[27:16]	0	
Reserved	[15:12]	0	
yvcoef1	[11:0]	0	

7.7.8.7 YV2_3 (YV2_3:0x6204)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yvcoef2[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	yvcoef2[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				yvcoef3[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	yvcoef3[7:0]							
Type	R/W							
Default	0							

Table 7-121

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yvcoef2	[27:16]	0	
Reserved	[15:12]	0	
yvcoef3	[11:0]	0	

7.7.8.8 YVm_n (m_n = 4_5 .. 122_123) (YVm_n:0x6208 – 0x62F4)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yvcoef m[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	yvcoef m[7:0]							
Type	R/W							

Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				yvcoef n[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	yvcoef n[7:0]							
Type	R/W							
Default	0							

Table 7-122

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yvcoef m	[27:16]	0	
Reserved	[15:12]	0	
yvcoef n	[11:0]	0	

7.7.8.9 YV124_125 (YV124_125:0x62F8)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yvcoef124[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	yvcoef124[7:0]							
Type	R/W							
Default	0							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved[3:0]				yvcoef125[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	yvcoef125[7:0]							
Type	R/W							
Default	0							

Table 7-123

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yvcoef124	[27:16]	0	
Reserved	[15:12]	0	
yvcoef125	[11:0]	0	

7.7.8.10 YV126_127 (YV126_127:0x62FC)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				yvcoef126[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	yvcoef126[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				yvcoef127[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	yvcoef127[7:0]							
Type	R/W							
Default	0							

Table 7-124

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
yvcoef126	[27:16]	0	
Reserved	[15:12]	0	
yvcoef127	[11:0]	0	

7.7.8.11 CH0_1 (CH0_1:0x6300)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				chcoef0[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	chcoef0[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				chcoef1[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	chcoef1[7:0]							
Type	R/W							
Default	0							

Table 7-125

Register Field	Bit	Default	Description

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
chcoef0	[27:16]	0	Cb/Cr horizontal coefficient #0
Reserved	[15:12]	0	
chcoef1	[11:0]	0	Cb/Cr horizontal coefficient #1

7.7.8.12 CH2_3 (CH2_3:0x6304)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				chcoef2[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	chcoef2[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				chcoef3[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	chcoef3[7:0]							
Type	R/W							
Default	0							

Table 7-126

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
chcoef2	[27:16]	0	Cb/Cr horizontal coefficient #2
Reserved	[15:12]	0	
chcoef3	[11:0]	0	Cb/Cr horizontal coefficient #3

7.7.8.13 CHm_n (m_n = 4_5..122_123) (CHm_n:0x6308 – 0x63F4)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				chcoef m[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	chcoef m[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				chcoef n[11:8]			
Type	RO				R/W			
Default	0				0			

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	chcoef n[7:0]							
Type	R/W							
Default	0							

Table 7-127

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
chcoef m	[27:16]	0	Cb/Cr horizontal coefficient #m
Reserved	[15:12]	0	
chcoef n	[11:0]	0	Cb/Cr horizontal coefficient #n

7.7.8.14 CH124_125 (CH124_125:0x63F8)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				chcoef124[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	chcoef124[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				chcoef125[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	chcoef125[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
chcoef124	[27:16]	0	Cb/Cr horizontal coefficient #124
Reserved	[15:12]	0	
chcoef125	[11:0]	0	Cb/Cr horizontal coefficient #125

7.7.8.15 CH126_127 (CH126_127:0x63FC)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				chcoef126[11:8]			
Type	RO				R/W			

Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	chcoef126[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				chcoef127[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	chcoef127[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
chcoef126	[27:16]	0	Cb/Cr horizontal coefficient #126
Reserved	[15:12]	0	
chcoef127	[11:0]	0	Cb/Cr horizontal coefficient #127

7.7.8.16 CV0_1 (CV0_1:0x6400)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				cvcoef0[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	cvcoef0[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				cvcoef1[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cvcoef1[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
cvcoef0	[27:16]	0	Cb/Cr vertical coefficient #0
Reserved	[15:12]	0	

cvcoef1	[11:0]	0	Cb/Cr vertical coefficient #1

7.7.8.17 CV2_3 (CV2_3:0x6404)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				cvcoef2[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	cvcoef2[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				cvcoef3[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cvcoef3[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
cvcoef2	[27:16]	0	Cb/Cr vertical coefficient #2
Reserved	[15:12]	0	
cvcoef3	[11:0]	0	Cb/Cr vertical coefficient #3

7.7.8.18 CVm_n (m_n = 4_5..122_123) (CVm_n:0x6408 – 0x64F4)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				cvcoef m[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	cvcoef m[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				cvcoef n[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	cvcoef n[7:0]							
Type	R/W							
Default	0							

Table 7-128

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
cvcoef m	[27:16]	0	Cb/Cr vertical coefficient #m
Reserved	[15:12]	0	
cvcoef n	[11:0]	0	Cb/Cr vertical coefficient #n

7.7.8.19 CV124_125 (CV124_125:0x64F8)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				cvcoef124[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	cvcoef124[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				cvcoef125[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cvcoef125[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
cvcoef124	[27:16]	0	Cb/Cr vertical coefficient #124
Reserved	[15:12]	0	
cvcoef125	[11:0]	0	Cb/Cr vertical coefficient #125

7.7.8.20 CV126_127 (CV126_127:0x64FC)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				cvcoef126[11:8]			

Type	RO				R/W			
Default	0				0			
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	cvcoef126[7:0]							
Type	R/W							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[3:0]				cvcoef127[11:8]			
Type	RO				R/W			
Default	0				0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cvcoef127[7:0]							
Type	R/W							
Default	0							

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
cvcoef126	[27:16]	0	Cb/Cr vertical coefficient #126
Reserved	[15:12]	0	
cvcoef127	[11:0]	0	Cb/Cr vertical coefficient #127

7.7.9 VIP and PP FIFO Registers

7.7.9.1 VIP_FIFO_PIXEL (VIP_FIFO_PIXEL:0x6524)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				vip_fifo_pixel[27:24]			
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	vip_fifo_pixel[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	vip_fifo_pixel[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	vip_fifo_pixel[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 7-129 VIP_FIFO_PIXEL

Register Field	Bit	Default	Description

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
vip_fifo_pixel	[27:0]	0	VIP FIFO PIXEL

7.7.9.2 PP_FIFO_PIXEL (PP_FIFO_PIXEL:0x6528)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved[3:0]				pp_fifo_pixel[27:24]			
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	pp_fifo_pixel[23:16]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	pp_fifo_pixel[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	pp_fifo_pixel[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 7-130 PP_FIFO_PIXEL

Register Field	Bit	Default	Description
Reserved	[31:28]	0	
pp_fifo_pixel	[27:0]	0	PP FIFO PIXEL

7.8 Internal Color Bar Generator

7.8.1 Debug Data Register (DB_Data: 0x7000)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	db_wdata[31:24]							
Type	WO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	db_wdata[23:16]							
Type	WO							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	db_wdata[15:8]							
Type	WO							
Default	0x00							

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	db_wdata[7:0]							
Type	WO							
Default	0x00							

Register Field	Bit	Description
db_wdata	[31:0]	**Debug Write Data** This data is used to write to the VB_FIFO in debug mode. Data is used as packed data and is repeated for subsequent addresses. For first location, db_wdata[31:0] = {B1,R0,G0,B0}……

7.8.2 Debug Control Register (DB_Ctl: 0x7080)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					db_clko	Reserved	
Type	RO					R/W	RO	
Default	0x0					0x0	0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	WC_src	Reserved					db_Vbuf	db_En
Type	R/W	RO					R/W	R/W
Default	0x0	0x0					0x0	0x0

Register Field	Bit	Description
Reserved	[15:11]	
db_clko	[10]	**DB_ClkO** 0: Normal Operation 1: Output TMDS clk to A_SCK pin Output CSI-2 Byte clk to A_WFS pin Output PHYCLK to A_SD[0] pin Output APLL clock to A_OSCK pin
Reserved	[9:8]	
WC_src	[7]	**Video Word count enable** 0: Taken from HDMI Rx (no scalar involved) 1: used Video word count register from 0x000A
Reserved	[6:2]	
db_VBuf	[1]	**Debug Video Buffer** 0: normal 1: enable I2C write to VB sram
db_CSI-2Txt	[0]	**Debug CSI-2 Block enable** 0: Normal mode 1: Debug mode

7.8.3 HD Self Check Register1 (SchkReg1: 0x7084)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	hpdi_st	hpdi_tg	ir_st	ir_tg	cec_st	cec_tg	test_st	rst_tg
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	x	x	x	x	x	x	x	x

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		hrx_opt	hrx_match	hrx_stst			stst_en
Type	RO		RO	RO	R/W			R/W
Default	0x0		0x0	0x0	0x0			0x0

Table 7-131 Self Check Register1

Register Field	Bit	Description
hdpi_st	[15]	HPDI pin status
hdpi_tg	[14]	HPDI toggle status
ir_st	[13]	IR Pin status
ir_tg	[12]	IR toggle status 0: not toggle 1: detect IR toggle
cec_st	[11]	CEC Pin status
cec_tg	[10]	CEC toggle status 0: not toggle 1: detect CEC toggle
test_st	[9]	TEST Pin status Read TEST pin status
rst_tg	[8]	RESETN toggle status 0: Not toggle 1: Toggle Must Write"1" first then toggle RESET pin
Reserved	[7:6]	
hrx_opt	[5]	HDMI Phy Test Status2 0: Select single mode compare 1: Select loop mode compare
hrx_match	[4]	HDMI Phy Test Status1 0: No match 1: Match
hrx_stst	[3:1]	HDMI Phy Self check enable 3'b000: Disable 3'b111: Enable self check test Bit[0] Enable HDMI Data 0 self check test Bit[1] Enable HDMI Data 1 self check test Bit[2] Enable HDMI Data 2 self check test HDMI Host must output the follow pattern pn7 1st cycle DATA[9:0] = 10'b00_0000_0000 2nd cycle DATA[9:0] = 10'b11_1111_1111 3rd cycle DATA[9:0] = 10'b00_0000_0000 4th cycle DATA[9:0] = 10'b00_0000_0001 5th cycle DATA[9:0] = 10'b00_0000_0010 6th cycle DATA[9:0] = 10'b00_0000_0100 7th cycle DATA[9:0] = 10'b00_0000_1000 8th cycle DATA[9:0] = 10'b00_0001_0000 9th cycle DATA[9:0] = 10'b00_0010_0000 10th cycle DATA[9:0] = 10'b00_0100_0000 11th cycle DATA[9:0] = 10'b00_1000_0000

		12th cycle DATA[9:0] = 10'b01_0000_0000 13th cycle DATA[9:0] = 10'b10_0000_0000 14th cycle DATA[9:0] = 10'b11_1111_1111 15th cycle DATA[9:0] = 10'b01_0101_0101 16th cycle DATA[9:0] = 10'b10_1010_1010 and loop back to 1st cycle DATA
stst_en	[0]	Self Check Enable 0: Disable 1: Enable

7.8.4 TC3587749 Self Check Register2 (SchkReg2: 0x7086)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	asc_d							
Type	R/W							
Default	0x5A							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	ddc_st							
Type	RO							
Default	0x0							

Table 7-132 Self Check Register1

Register Field	Bit	Description
asc_d	[15:8]	Audio Self Check Data - Channel 0 Left data = {asc_d,asc_d,asc_d,asc_d} - Channel 0 Right data = Inverted of Channel 0 Left data - Channel 1 Left data = Channel 0 Left data shift left by 1 (MSB → LSB) - Channel 1 Right data = Inverted Channel 1 Left data - Channel 2 Left data = Channel 1 Left data data shift left by 1 (MSB → LSB) - Channel 2 Right data = Inverted Channel 1 Left data - Channel 3 Left data = Channel 2 Left data shift left by 1 (MSB → LSB) - Channel 3 Right data = Inverted Channel 1 Left data
ddc_st	[7:0]	DDC first byte status

7.8.5 Debug Active Line Count Register (DAVLCreg: 0x7090)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					db_alcnt[10:8]		
Type	RO					R/W		
Default	0x0					0x1		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	db_alcnt[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[15:11]	
db_alcnt	[10:0]	Debug Active Line Count 10'h0: 1 line 10'h1: 2 line .. 11'h7FF: 2048 lines

7.8.6 Debug Line Width Register (DAWCreg: 0x7092)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved			db_awcnt[12:8]				
Type	RO			R/W				
Default	0x0			0x1				
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	db_awcnt[7:0]							
Type	R/W							
Default	0x0							

Register Field	Bit	Description
Reserved	[15:12]	
db_width	[12:0]	Debug Total byte count in a line (include blank period) 13'h0: 1 byte 13'h1: 2 bytes .. 13'h1FFF: 8192 bytes Note that there is only a maximum of 4096 byte of storage for color bar. Therefore, only YCbCr422 8-bit (1920 x 2 bytes per pixel = 3840 bytes) is supported for 1080p color bar.

7.8.7 Debug Vertical Blank Line Count Register (DVBCreg: 0x7094)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	db_vb[6:0]						
Type	RO	R/W						
Default	0x0	0x10						

Register Field	Bit	Description
Reserved	[15:7]	
db_vb	[6:0]	Debug Vertical Blank line 7'h0: 1 line

Register Field	Bit	Description
		7'h1: 2 line .. 7'7F:128 line

7.9 HDMI Rx System Control

7.9.1 HDMI Rx Interrupt Registers

7.9.1.1 INTERRUPT0 REGISTER (HDMI_INT0) (0x8500)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_KEY	Reserved					I_MISC	I_PHYERR
Type	RO	RO					RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_KEY	7	0	KEY-EDID (address 0x85_0F) interrupt 0: No interrupt, 1: Interrupt generated
I_MISC	1	0	MISC (address 0x85_0B) interrupt 0: No interrupt, 1: Interrupt generated
I_PHYERR	0	0	PHY-ERR (address 0x85_0A) interrupt 0: No interrupt, 1: Interrupt generated

7.9.1.2 INTERRUPT1 REGISTER (HDMI_INT1) (0x8501)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_GBD	I_HDCP	I_ERR	I_AUD	I_CBIT	I_PACKET	I_CLK	I_SYS
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_GBD	7	0	GBD (address 0x85_09) interrupt 0: No interrupt, 1: Interrupt generated
I_HDCP	6	0	HDCP (address 0x85_08) interrupt 0: No interrupt, 1: Interrupt generated
I_ERR	5	0	ERR (address 0x85_07) interrupt 0: No interrupt, 1: Interrupt generated
I_AUD	4	0	Audio Buffer (address 0x85_06) interrupt 0: No interrupt, 1: Interrupt generated

I_CBIT	3	0	Audio CBIT (address 0x85_05) interrupt 0: No interrupt, 1: Interrupt generated
I_PACKET	2	0	Info Packet (address 0x85_04) interrupt 0: No interrupt, 1: Interrupt generated
I_CLK	1	0	Pixel CLK (address 0x85_03) interrupt 0: No interrupt, 1: Interrupt generated
I_SYS	0	0	SYSTEM (address 0x85_02) interrupt 0: No interrupt, 1: Interrupt generated

7.9.1.3 SYSTEM INTERRUPT (SYS_INT) (0x8502)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_ACR_CTS	I_ACRN	I_DVI	I_HDMI	I_NOPMBDET	I_DPMBDET	I_TMDS	I_DDC
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_ACR_CTS	7	0	Receive CTS update interrupt 0: No interrupt 1: Interrupt generated
I_ACRN	6	0	Receive N update interrupt 0: No interrupt 1: Interrupt generated
I_DVI	5	0	HDMI→DVI change detection interrupt 0: No interrupt 1: Interrupt generated
I_HDMI	4	0	DVI→HDMI change detection interrupt 0: No interrupt 1: Interrupt generated
I_NOPMBDET	3	0	No DataIsland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_DPMBDET	2	0	With DataIsland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDS	1	0	TMDS amplitude change interrupt 0: No interrupt 1: Presence change detected (PHY squelch ON/OFF changedetected)
I_DDC	0	0	DDC power change detection interrupt 0: No interrupt 1: 0V⇔5V change detected

7.9.1.4 CLOCK INTERRUPT (CLK_INT) (0x8503)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	I_OUT_H_CHG	I_IN_DE_CHG	I_IN_HV_CHG	I_DC_CHG	I_PXCLK_CHG	I_PHYCLK_CHG	I_TMDSCLK_CHG
Type	R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	x	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	7	0	
I_OUT_H_CHG	6	0	(Output side) H counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_IN_DE_CHG	5	0	(Input side) DE size and position change detection interrupt 0: No interrupt 1: Interrupt generated
I_IN_HV_CHG	4	0	(Input side) HV counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_CHG	3	0	Deep Color mode change detection interrupt 0: No interrupt 1: Interrupt generated
I_PXCLK_CHG	2	0	Pixel CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_PHYCLK_CHG	1	0	PHY PLL CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDSCLK_CHG	0	0	TMDS CLK change detection interrupt 0: No interrupt 1: Interrupt generated

7.9.1.5 PACKET INTERRUPT (PACKET_INT) (0x8504)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_PK_ISRC2	I_PK_ISRC	I_PK_ACP	I_PK_VS	I_PK_SPD	I_PK_MS	I_PK_AUD	I_PK_AVI
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_PK_ISRC2	7	0	ISRC2 packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_ISRC	6	0	ISRC1 packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_ACP	5	0	ACP packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_VS	4	0	861B VS_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_SPD	3	0	861B SPD_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_MS	2	0	861B MS_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_AUD	1	0	861B AUD_info packet update interrupt 0: No interrupt, 1: Interrupt generated
I_PK_AVI	0	0	861B AVI_info packet update interrupt 0: No interrupt, 1: Interrupt generated

※ Interrupt is generated only when receive content has changed.
If the same data is repeatedly received, interrupt is not generated.

7.9.1.6 CBIT INTERRUPT (CBIT_INT) (0x8505)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_AF_LOCK	I_AF_UNLOCK	I_AU_DST	I_AU_DSD	I_AU_HBR	I_CBIT_NLPCM	I_CBIT_FS	I_CBIT
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AF_LOCK	7	0	Audio clock frequency lock detection interrupt 0: No interrupt 1: Interrupt generated
I_AF_UNLOCK	6	0	Audio clock frequency unlock detection interrupt 0: No interrupt

			1: Interrupt generated
I_AU_DST	5	0	DST packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_DSD	4	0	DSD packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_HBR	3	0	HBR packet detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_NLPCM	2	0	Normal Audio LPCM⇔NLPCM change detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_FS	1	0	Receive data F_S update interrupt 0: No interrupt 1: Interrupt generated
I_CBIT	0	0	Receive C_bit data [47:0] update interrupt 0: No interrupt 1: Interrupt generated

7.9.1.7 AUDIO INTERRUPT (AUDIO_INT) (0x8506)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_BUF_OVER	I_BUF_NO2	I_BUF_NO1	I_BUF_CENTER	I_BUF_NU1	I_BUF_NU2	I_BUF_UNDER	I_BUFINIT_END
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_BUF_OVER	7	0	Buffer Over flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO2	6	0	Buffer Nearly Over (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO1	5	0	Buffer Nearly Over (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated

I_BUF_CENTER	4	0	Buffer CENTER detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NU1	3	0	Buffer Nearly Under (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NU2	2	0	Buffer Nearly Under (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_UNDER	1	0	Buffer Under flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUFINIT_END	0	0	Buffer initial operation completed interrupt 0: No interrupt 1: Interrupt generated

7.9.1.8 ERROR INTERRUPT (ERR_INT) (0x8507)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_EESS_ERR	I_AU_FRAME	I_NO_ACP	I_NO_AVI	I_DC_NOCD	I_DC_DEERR	I_DC_BUFERR	I_DC_PPERR
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_EESS_ERR	7	0	EESS error generation detection interrupt ※1 [6] W1C/R 1'b0 0: No interrupt 1: Interrupt generate
I_AU_FRAME	6	0	60958Frame discontinuous change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_ACP	5	0	ACP Packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_AVI	4	0	AVI Packet receive cut detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_NOCD	3	0	Deep Color CD=0 (or not defined) generates 24bit mode auto move 0: No interrupt 1: Interrupt generated
I_DC_DEERR	2	0	In Deep Color Packing Group, DE position abnormal generation 0: No interrupt 1: Interrupt generated

I_DC_BUFERR	1	0	Deep Color FIFO flow generation 0: No interrupt 1: Interrupt generated
I_DC_PPERR	0	0	Deep Color UnPack phase dis-unified generation 0: No interrupt 1: Interrupt generated

※1 During HDMI(=EESS) mode, detects state where Enc_Disable、Enc_Enable can no longer be detected during HDCP decoding operation.
Used for detecting the abnormal state where HDCP goes OFF without te send side sending Enc_Disable.

7.9.1.9 HDCP INTERRUPT (HDCP_INT) (0x8508)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_AVM_SET	I_AVM_CLR	I_LINKERR	I_SHA_END	I_R0_END	I_KM_END	I_AKSV_END	I_AN_END
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AVM_SET	7	0	SET AVMUTE receive interrupt 0: No receive, 1: With receive
I_AVM_CLR	6	0	CLRAE AVMUTE receive interrupt 0: No receive, 1: With receive
I_LINKERR	5	0	Link error detection interrupt ※1 0: No link error 1: Link error generated
I_SHA_END	4	0	V´value operation ended interrupt 0: During idle or operation 1: Operation ended
I_R0_END	3	0	Ks´, M0´, R0´ operation ended interrupt 0: During idle or operation 1: Operation ended
I_KM_END	2	0	Km´ operation ended interrupt 0: During idle or operation 1: Operation ended
I_AKSV_END	1	0	AKSV write completed interrupt 0: During idle or write 1: Write completed notification
I_AN_END	0	0	AN write completed interrupt 0: During idle or write 1: Write completed notification

※1 This interrupt is generated when other device termination of HDCP encoding is detected. (Detects IDLE State after HDCP certification No.3 part)
However, it may be set up even during HDMI SET_AVMUTE.

7.9.1.10 GBD INTERRUPT (GBD_INT) (0x8509)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_GBD_PKERR	I_GBD_ACLR	I_P1GBD_CHG	I_P0GBD_CHG	Reserved	I_P1GBD_DET	I_GBD_OFF	I_GBD_ON
Type	W1C/R	W1C/R	W1C/R	W1C/R	RO	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_GBD_PKERR	7	0	GBD packet receive ERR generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ACLR	6	0	GBD packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated (cutoff generated)
I_P1GBD_CHG	5	0	Valid P1 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM update generated)
I_P0GBD_CHG	4	0	Valid P0 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM updategenerated)
I_P1GBD_DET	2	0	P1 GBD data receive generation interrupt 0: No interrupt 1: Interrupt generated 【Note】 Not related to change in packet content, generated each time packet is received.
I_GBD_OFF	1	0	Valid GBD yes→no change generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ON	0	0	Valid GBD no→yes change generation interrupt 0: No interrupt 1: Interrupt generated

7.9.1.11 MISC INTERRUPT (MISC_INT) (0x850b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			I_AS_LAYOUT	I_NO_SPD	I_NO_VS	I_SYNC_CHG	I_AUDIO_MUTE
Type	RO			W1C/R	W1C/R	W1C/R	W1C/R	W1C/R

Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AS_LAYOUT	4	0	audio Layout Bit change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_SPD	3	0	SPD_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_VS	2	0	VS_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_SYNC_CHG	1	0	Video sync signal state change detection interrupt 0: No interrupt 1: Interrupt generated
I_AUDIO_MUTE	0	0	Audio MUTE generation interrupt 0: No interrupt 1: Interrupt generated

7.9.1.12 KEY INTERRUPT (KEY_INT) (0x850f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				I_BKSV_ERR	I_KD_RDEND	I_KD_RSTEND	I_KD_ERR
Type	RO				RO	W1C/R	W1C/R	W1C/R
Default	0x0				0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:4]	0	
I_BKSV_ERR	3	0	BKSV data check error interrupt (1/0 number) 0: No error 1: Error generation notification
I_KD_RDEND	2	0	Device key forward completed interrupt ※1 0: During idle or forwarding 1: Forward completed notification
I_KD_RSTEND	1	0	KEY-EEPROM reset operation completed interrupt 0: During idle or reset operation 1: Reset completed notification
I_KD_ERR	0	0	KEY-EEPROM ACK error interrupt 0: No error 1: Error generation notification (No slave address ACK from Key EEPROM)

7.9.1.13 SYS INTERRUPT MASK (SYS_INTM) (0x8512)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_ACR_CTS	M_ACR_N	M_DVI_DET	M_HDMI_DET	M_NOPMBDET	M_BPMBDET	M_TMDS	M_DDC
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_ACR_CTS	7	1	Receive CTS update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_ACR_N	6	1	Receive N value update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DVI_DET	5	1	HDMI→DVI change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_HDMI_DET	4	1	DVI→HDMI change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NOPMBDET	3	1	No DataIsland Preamble detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BPMBDET	2	1	With DataIsland Preamble detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_TMDS	1	1	TMDS amplitude change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DDC	0	1	DDC power change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.14 CLK INTERRUPT MASK (CLK_INTM) (0x8513)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	M_OUT_H_CHG	M_IN_DE_CHG	M_IN_HV_CHG	M_DC_CHG	M_PXCLK_CHG	M_PHYCLK_CHG	M_TMDS_CHG
Type	R	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
Reserved	7	1	
M_OUT_H_CHG	6	1	(Output side) H counter change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_IN_DE_CHG	5	1	(Input side) DE size and position change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_IN_HV_CHG	4	1	(Input side) HV counter change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_CHG	3	1	Deep Color change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PXCLK_CHG	2	1	Pixel CLK change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PHYCLK_CHG	1	1	PHY PLL CLK change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_TMDS_CHG	0	1	TMDS CLK change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.15 PACKET INTERRUPT MASK (PACKET_INTM) (0x8514)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_PK_ISRC2	M_PK_ISRC	M_PK_ACP	M_PK_VS	M_PK_SPD	M_PK_MS	M_PK_AUD	M_PK_AVI
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_PK_ISRC2	7	1	ISRC2 packet receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_ISRC	6	1	ISRC1 packet receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_ACP	5	1	ACP packet receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_PK_VS	4	1	861B VS_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_SPD	3	1	861B SPD_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_MS	2	1	861B MS_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_AUD	1	1	861B AUD_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_PK_AVI	0	1	861B AVI_info packet update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.16 CBIT INTERRUPT MASK (CBIT_INTM) (0x8515)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_AF_LOCK	M_AF_UNLOCK	M_AU_DST	M_AU_DSD	M_AU_HBR	M_CBIT_NLPCM	M_CBIT_FS	M_CBIT
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_AF_LOCK	7	1	Audio clock frequency lock detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AF_UNLOCK	6	1	Audio clock frequency unlock detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_DST	5	1	DST Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_DSD	4	1	DSD Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_HBR	3	1	HBR Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT_NLPCM	2	1	Receive data LPCM⇔NLPCM change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_CBIT_FS	1	1	Receive data F_S update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT	0	1	Receive C_bit data [39:0] update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.17 AUDIO INTERRUPT MASK (AUDIO_INTM) (0x8516)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_BUF_OVER	M_BUF_NO2	M_BUF_NO1	M_BUF_CENTER	M_BUF_NU1	M_BUF_NU2	M_BUF_UNDER	M_BUFINIT_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_BUF_OVER	7	1	Buffer Over flow detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NO2	6	1	Buffer Nearly Over (Threshold 2) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NO1	5	1	Buffer Nearly Over (Threshold 1) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_CENTER	4	1	Buffer CENTER detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NU1	3	1	Buffer Nearly Under (Threshold 1) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_NU2	2	1	Buffer Nearly Under (Threshold 2) detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUF_UNDER	1	1	Buffer Under flow detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_BUFINIT_END	0	1	Buffer initialization operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.18 ERR INTERRUPT MASK (ERR_INTM) (0x8517)

Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	M_EESS_ERR	M_AU_FRAME	M_NO_ACP	M_NO_AVI	M_DC_NOCD	M_DC_DEERR	M_DC_BUFERR	M_DC_PPERR
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_EESS_ERR	7	1	EESS error occurrence detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_FRAME	6	1	Audio 60958Frame discontinuous detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NO_ACP	5	1	ACP packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NO_AVI	4	1	AVI packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_NOCD	3	1	Deep color 24bit mode auto move occurrence interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_DEERR	2	1	In Deep Color Packing Group, DE position abnormal occurrencinterrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_BUFERR	1	1	Deep Color FIFO flow occurrence interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_DC_PPERR	0	1	Deep Color UnPack phase dis-unify occurrence 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.19 HDCP INTERRUPT MASK (HDCP_INTM) (0x8518)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_AVM_SET	M_AVM_CLR	M_LINKERR	M_SHA_END	M_R0_END	M_KM_END	M_AKSV_END	M_AN_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_AVM_SET	7	1	SET AVMUTE receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_AVM_CLR	6	1	CLRAE AVMUTE receive interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_LINKERR	5	1	Link error detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_SHA_END	4	1	V´ value operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_R0_END	3	1	Ks´, M0´, R0´ operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_KM_END	2	1	Km´ operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AKSV_END	1	1	AKSV write completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AN_END	0	1	AN write completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.20 GBD INTERRUPT MASK (GBD_INTM) (0x8519)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_GBD_PKERR	M_GBD_ACLR	M_P1GBD_CHG	M_P0GBD_CHG	Reserved	M_P1GBD_DET	M_GBD_OFF	M_GBB_ON
Type	RW	RW	RW	RW	RO	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_GBD_PKERR	7	1	GBD packet receive error occurrence interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_GBD_ACLR	6	1	GBD packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_P1GBD_CHG	5	1	P1 GBD update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_P0GBD_CHG	4	1	P0 GBD update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

M_P1GBD_DET	2	1	P1 GBD data receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_GBD_OFF	1	1	No Valid GBD detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_GBB_ON	0	1	With valid GBD detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.21 MISC INTERRUPT MASK (MISC_INTM) (0x851b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			M_AS_LAYOUT	M_NO_SPD	M_NO_VS	M_SYNC_CHG	M_AUDIO_MUTE
Type	RO			RW	RW	RW	RW	RW
Default	0	0	0	1	1	1	1	1

Register Field	Bit	Default	Description
M_AS_LAYOUT	4	1	audio Layout Bit change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NO_SPD	3	1	SPD_Info packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_NO_VS	2	1	VS_Info packet receive cutoff detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_SYNC_CHG	1	1	Video sync signal state change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AUDIO_MUTE	0	1	Audio MUTE generation interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.1.22 KEY INTERRUPT MASK (KEY_INTM) (0x851f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				M_BKSV_ERR	M_KD_RDEND	M_KD_RSTEND	M_KD_ERR
Type	RO				RW	RW	RW	RW
Default	0xF				1	1	1	1

Register Field	Bit	Default	Description
Reserved	[7:4]	0xF	

M_BKSV_ERR	3	1	BKSV data check error interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_KD_RDEND	2	1	Device key forward command completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_KD_RSTEND	1	1	KEY-EEPROM reset operation completed interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_KD_ERR	0	1	KEY-EEPROM ACK error interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

7.9.2 HDMI Rx Status Registers

7.9.2.1 SYS STATUS (SYS_STATUS) (0x8520)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_SYNC	S_AVMUTE	S_HDCP	S_HDMI	S_PHY_SCDT	S_PHY_PLL	S_TMDS	S_DDC5V
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_SYNC	7	0	Input Video sync signal status 0 : No sync signal (unstable) 1: With sync signal (stable)
S_AVMUTE	6	0	AVMUTE status 0: AVMUTE=OFF 1: AVMUTE=ON
S_HDCP	5	0	HDCP status 0: HDCP=OFF (no code) 1: HDCP=ON (with code)
S_HDMI	4	0	HDMI status 0: DVI 1: HDMI
S_PHY_SCDT	3	0	PHY DE detect status (PHY SCDT signal monitor) 0: No DE 1: With DE
S_PHY_PLL	2	0	PHY PLL status (PHY PLL_LOCK_IND signal monitor) 0: UnLock 1: Lock
S_TMDS	1	0	TMDS input amplitude status (PHY squelch signal monitor) 0: No input amplitude, 1: With input amplitude
S_DDC5V	0	0	DDC_Power (DDC5V) input status 0: No input, 1: With input

7.9.2.2 VIDEO INPUT STATUS (VI_STATUS) (0x8521)

Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	S_V_repeat				S_V_format			
Type	RO				RO			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_repeat	7:4	0	Input Video signal status (Repetition) 0: No Repetition, 1: Repetition = 2, 2: Repetition = 3, 3: Repetition = 4, ・・・・, 9: Repetition = 10
S_V_format	3:0	0	Video format status detected from input DE size ※Shows the status before implementation of correction using repetition. 4'd1 : VGA (Horizontal 631～649, Vertical 471～489) 4'd2 : 240p/480i (Horizontal 1401～1449, Vertical 231～249) 4'd3 : 288p/576i (Horizontal 1401～1449, Vertical 279～297) 4'd4 : W240p/480i (Horizontal 2801～2899, Vertical 231～249) 4'd5 : W288p/576i (Horizontal 2801～2899, Vertical 279～297) 4'd6 : 480p (Horizontal 701～729, Vertical 471～489) 4'd7 : 576p (Horizontal 701～729, Vertical 567～585) 4'd8 : W480p (Horizontal 1401～1449, Vertical 471～489) 4'd9 : W576p (Horizontal 1401～1449, Vertical 567～585) 4'd10 : WW480p (Horizontal 2801～2899, Vertical 471～489) 4'd11 : WW576p (Horizontal 2801～2899, Vertical 567～585) 4'd12 : 720p (Horizontal 1261～1289, Vertical 711～729) 4'd13 : 1035i (Horizontal 1911～1929, Vertical 507～527) 4'd14 : 1080i (Horizontal 1911～1929, Vertical 531～549) 4'd15 : 1080p (Horizontal 1911～1929, Vertical 1071～1089) 4'd0 : Other than above

7.9.2.3 VIDEO INPUT STATUS1 (VI_STATUS1) (0x8522)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_GBD	Reserved			S_DeepColor		S_V_422	S_V_interlace

Type	RO	RO			RO		RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_GBD	6:4	0	Effective GBD data status ※1 0: No GBD, 1: With GBD
	3:2		Reserved
S_V_422	1	0	Input Video signal status (422 detection) ※3 0 : 444, 1 : 422
S_V_interlace	0	0	Input Video signal status (Interlace detection) ※4 0: Progressive, 1: Interlace

※1 During DVI input, judged to be No GBD.
※2 During DVI input, judged to be 24bit.
※3 During DVI input, judged to be 444. During HDMI input, judged from the AVI-Info value.
※4 Progressive/Interlace judgment method follows the address0x858e[4]bit setting.

7.9.2.4 AUDIO STATUS0 (AU_STATUS0) (0x8523)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_A_MUTE			S_A_DST	S_A_DSD	S_A_HBR	S_A_NLPCM	S_A_sample
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_A_MUTE	7	0	AUDIO auto mute status 0: Mute OFF, 1: Mute ON
	6:5	0	Reserved
S_A_DST	4	0	Compressed 1BIT Audio packet transmission status (1.5msec update) 0: No DST transmission, 1: With DST transmission
S_A_DSD	3	0	1BIT Audio packet transmission status (1.5msec update) 0: No DSD transmission, 1: With DSD transmission
S_A_HBR	2	0	HBR Audio packet transmission status (1.5msec update) 0: No HBR transmission, 1: With HBR transmission
S_A_NLPCM	1	0	Normal AUDIO/HBR AUDIOpacket compression stream detection 0: LPCM, 1: Compression stream (61937-1

S_A_sample	0	0	Normal AUDIO packet transmission status (1.5msec update) 0: No AUDIO transmission, 1: With AUDIO transmission

7.9.2.5 AUDIO STATUS1 (AU_STATUS1) (0x8524)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	3D_STRUCURE				S_VS	S_SPD	S_PKERR	S_ACP
Type	RO				RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
3D_STRUCURE	7:4	0	3D transmission format information in VS info 0000: Frame packing 0001 Field alternative 0010: Line alternative 0011: Side-by-Side(Full) 0100: L + depth 0101: L + depth + graphics + graphics-depth 0110: Top-and-Bottom 0111: Reserved 1000: Side-by-Side(Half) 1001-1110: Reserved 1111: Not used ※Valid when S_VS_VIC_3D(0x8525[5]) is 1
S_VS	3	0	VS packet transmission status 0: No VS transmission, 1: With VS transmission
S_SPD	2	0	SPD packet transmission status 0: No SPD transmission, 1: With SPD transmission
S_PKERR	1	0	Packet receive error occurrence status 0: No Packet receive error, 1: Packet receive error now occurring
S_ACP	0	0	ACP packet transmission status 0: No ACP transmission, 1: With ACP transmission

7.9.2.6 VIDEO INPUT STATUS2 (VI_STATUS2) (0x8525)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_FP_IP		S_VS_VIC	S_422out	Reserved			S_DC_NO

			_3D					CD
Type	RO		RO	RO	RO			RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_FP_IP	7:6	0	IP judgment result 0x8980[2] due to size （Vertical V size andvertical DE size） or VIC to select whether to use size or VIC tojudge. Valid during Frame packing receive. 2'd0: Progressive 2'd1: Interlace 2'd2: VIC=39
S_VS_VIC_3D	5	0	3D format judgment result due to VS info ※ 0: Non-3D format 1: 3D format 【Note】Valid during HDMI input only. During DVI input, fixed at 0. When VS Info packet HDMI Video format(PB4 [7:5]) = 3'b010, set o 1.
S_422out	4	0	Current HDMI block Video output status 0: 444 output, 1:422 output
S_DC_NOCD	0	0	Status determining whether Color Depth used in current Deep Color unpack operation is in 24bit mode due to auto move 0: During normal operation (DVI mode or normal CD value) 1: CD=0 or CD=reserved or Operations due to No GC Packet

7.9.2.7 CLK STATUS (CLK_STATUS) (0x8526)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_3D_format						S_CLK_U21M	S_CLK_DC
Type	RO				RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_3D_format	7:4	0	3D Video format status detected from input DE size※1 4'd1 : 3D 1080i Frame Packing (Horizontal 1911～1929, Vertical 2219～2237) 4'd2 : 3D 1080p Frame Packing or L+depth (Horizontal 1911～1929, Vertical 2196～2214)

			4'd3 : 3D 720p Frame Packing or L+depth (Horizontal 1271～1289, Vertical 1461～1479) 4'd4 : 3D 1080p Line alternative (Horizontal 1911～1929, Vertical 2151～2169) 4'd5 : 3D 720p Line alternative (Horizontal 1271～1289, Vertical 1431～1449) 4'd6 : 3D 1080i Side by Side(Full) (Horizontal 3831～3849, Vertical 531～549) 4'd7 : 3D 1080p Side by Side(Full) (Horizontal 3831～3849, Vertical 1071～1089) 4'd8 : 3D 720p Side by Side(Full) (Horizontal 2551～2569, Vertical 711～729) 4'd9 : 3D 1080p L+depth+G+G_depth (Horizontal 1911～1929, Vertical 4446～4464) 4'd10 : 3D 720p L+depth+G+G_depth (Horizontal 1271～1289, Vertical 2961～2979) 4'd0 : Other than above
	3:2	0	
S_CLK_U21M	1	0	TMDS clock detection status at less than 21MHz 0: 21MHz or more , 1: Less than 21MHz
S_CLK_DC	0	0	TMDS clock DC condition detection status 0: Non DC condition, 1: DC condition 【Note】In reality, DC to frequency of about 1MHz or less is "1". Responds even when TMDS clock is not input (amplitude 0).

※1 3D 1080i Line alternative cannot identify 2D 1080p,
3D Side by Side (Half) cannot identify 2D format,
3D Top-and-Bottom cannot identify 2D format,
The ab ove unidentifiable format is displayed as 4'd0.

7.9.2.8 PHYERR STATUS (PHYERR_STATUS) (0x8527)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_TMDS_TG	S_3YNC_ERR	S_PIT_ERR	S_AT_ERR	S_CDR2_ERR	S_CDR1_ERR	S_CDR0_ERR	S_PLL_ERR
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_TMDS_TG	7	0	TMDS clock toggle detection 1: With toggle

S_3YNC_ERR	6	0	3ch sync error (risk phase) detection 1: Abnormal detection
S_PIT_ERR	5	0	PIT abnormal operation detection 1: Abnormal detection
S_AT_ERR	4	0	ATabnormal operation detection 1: Abnormal detection
S_CDR2_ERR	3	0	CH2 CDR abnormal detection 1: Abnormal detection
S_CDR1_ERR	2	0	CH1 CDR abnormal detection 1: Abnormal detection
S_CDR0_ERR	1	0	CH0 CDR abnormal detection 1: Abnormal detection
S_PLL_ERR	0	0	PLL lock removal detection 1: Abnormal detection

7.9.2.9 VI STATUS3 (VI_STATUS3) (0x8528)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			S_V_color				
Type	RO			RO				
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_color	4:0	0	Input Video signal color space judgment status ※1 5'b00 000 RGB (Full) 5'b00 001 RGB (Limitedl) 5'b00 010 YCbCr601 (Full) 5'b00 011 YCbCr601 (Limited) 5'b00 110 YCbCr709 (Full) 5'b00 111 YCbCr709 (Limited) 5'b00 100 Adobe_RGB (Full) 5'b00 101 Adobe_RGB (Limited) 5'b01 010 xvYCC601 (Full) 5'b01 011 xvYCC601 (Limited) 5'b01 110 xvYCC709 (Full) 5'b01 111 xvYCC709 (Limited) 5'b10 010 sYCC601 (Full) 5'b10 011 sYCC601 (Limited) 5'b11 010 Adobe_YCC601 (Full) 5'b11 011 Adobe_YCC601 (Limited) ※Values other than above are not generated 【Note】 Each bit has the following meaning. [0] Full/Limited identification bit [1] RGB/YCbCr identification bit [2] During RGB input, category identification bit

			During YCbCr input, 601/709 identification bi t [4: 3] During RGB input, 00 fixed During YCbCr input, category identification bit

※1 During DVI input, judged as RGB. For range identification, follow the address0x8570[3]bit setting. During HDMI input, judged from AVI-Info value. If at AVI-Info judged to be RGB, for the range identification follow the address0x8570[2]bit.

7.9.3 HDMI Rx Control Registers

7.9.3.1 PHY CONTROL0 (PHY_CTL0) (0x8531)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						PHY_SYS CLK_IND	PHY_CTL
Type	RO						R/W	RW
Default	0	0	1	0	0	0	1	0

Register Field	Bit	Default	Description
	7:1		Reserved
PHY_SYSCLK_IND	1	1	PHY System clock frequency setting 0: 27MHz 1: 42MHz
PHY_CTL	0	0	PHY power ON/OFF control mode 0: HOST manual setting 1: DDC5V detection operation (reaction time depends on address 0x8543[1:0] setting)

7.9.3.2 PHY ENABLE (PHY_EN) (0x8534)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							ENABLE_ PHY
Type	RO							RW
Default	0	0	1	1	1	1	1	1

Register Field	Bit	Default	Description
	7:1		Reserved
ENABLE_PHY	0	1	PHY general SUSPEND control ※2 ※3 0: Suspend 1: Normal Operation

※2 When PHY power ON/OFF control mode is for “HOST manual setting” (address0x85_31[0] == 0) only, Write is enabled in this register.
※3 When PHY power ON/OFF control mode is “DDC5V detect link” (address0x85_31[0] == 1), DDC5V input =H, and Suspend is automatically cleared.

7.9.3.3 PHY RESET (PHY_RST) (0x8535)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							RESET_CTRL
Type	RO							RW
Default	1	0	1	1	0	0	1	1

Register Field	Bit	Default	Description
	7:1		Reserved
RESET_CTRL	0	1	PHY general Reset control 0: Reset 1: Normal Operation

※1 There is no automatic clear function in this register.

7.9.3.4 PHY PLL (PHY_PLL) (0x8538)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PLL_CONFIG				PLL_CLK_RANGE			
Type	RW				RW			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
PLL_CONFIG	7:4	0	PHY PLL Band Width adjustment 0000 : 4MHz 0001 : 6MHz 0010 : 8MHz 0011 : 10MHz Other than above : TBD
PLL_CLK_RANGE	3:0	0	PHY PLL oscillation clock range setting 0000 : 0～36MHz, 0001 : 36～50MHz, 0010 : 50～70MHz, 0011 : 70～96MHz, 0100 : 96～140MHz, 0101 : 140～196MHz, 0110 : 196～246MHz, 0111 : 246MHz or more Other than above : TBD 【Note】 When in automatic switching

			mode(address0x8531[3] == 0), sinceHW is automatically set, write is impossible from the HOST.

7.9.3.5 PHY CDR (PHY_CDR) (0x853a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	CDR_SCALE			PI_CLK_RANGE			
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	1	0	0	0	0

Register Field	Bit	Default	Description
CDR_SCALE	6:4	0x1	PHY Phase interpolator step size 001 : default Other than above : TBD
PI_CLK_RANGE	3:0	0	PHY Phase interpolator clock range setting 0000 : 0～70MHz, 0001 : 70～170MHz, 0010 : 170～270MHz, 0011 : 270MHz or more Other than above : TBD 【Note】When in automatic switching mode (address0x8531[4] == 0), ince HW is automatically set, write is impossible from the HOST.

7.9.3.6 SYS FREQ0 Register (SYS_FREQ0) (0x8540)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ0							
Type	R/W							
Default	0x68							

Register Field	Bit	Default	Description
SYS_FREQ0	7:0	0x68	System clock frequency setting (lower bits) Set System clock frequency setting divide 10000 integer Ex. When system clock at 27MHz, 2700 = 16'h0A8C When system clock at 42MHz, 4200 = 16'h1068

7.9.3.7 SYS FREQ1 Register (SYS_FREQ1) (0x8541)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ1							
Type	R/W							
Default	0x10							

Register Field	Bit	Default	Description
SYS_FREQ1	7:0	0x10	System clock frequency setting (upper bits)

7.9.3.8 DDC CONTROL (DDC_CTL) (0x8543)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				DDC_ACK_POL	DDC_ACTION	DDC5V_MODE	
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	1	1	0	0	0	0

Register Field	Bit	Default	Description
	7:4		Reserved
DDC_ACK_POL	3	0	DDC_ACK output terminal polarity selection 0： H active output 1： L active output
DDC_ACTION	2	0	Selection of response method for DDC access from send side 0： Respond to DDC access only while HotPLUG is being output 1： Normally respond to DDC access when initialization completion flag=”1”
DDC5V_MODE	1:0	0	DDC5V_active detect delay setting To prevent chattering in the DDC5V input rising detection area, DDC5V is judged as avtime after a specified time from the rise detect point in time. 00: 0msec, 01: 50msec, 10: 100msec, 11: 200msec, 【Note】 With this setting, the DDC5V detection interrupt, HOTPLUG automatic output, and PHY automatic power ON timing are all

			delayed.

7.9.3.9 HPD Control Register (HPD_CTL) (0x8544)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HPD_CTL0	Reserved			HPD_OUT0
Type	RO				RO			
Default	0x0			0x0	0x0			0x0

Register Field	Bit	Default	Description
Reserved	7:5	0x0	
HPD_CTL0	4	0x0	HOTPLUG output ON/OFF control mode 0: Host manual setting 1: DDC5V detection interlock
Reserved	3:1	0x0	
HPD_OUT0	0	0x0	HOTPLUT Output setting 0: HOTPLUG = “L” output 1: HOTPLUG = “H” output Note: When at DDC5V detection interlock setting, write is not valid. Become status monitor bit.

7.9.3.10 ANA CONTROL (ANA_CTL) (0x8545)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		APLL_PCSX		Reserved			ANALOG_ON
Type	RO		RW		RO			RW
Default	0	0	0	1	0	0	0	0

Register Field	Bit	Default	Description
APLL_PCSX	5:4	0X1	PLL charge pump setting for Audio 00: HiZ, 01: L-fix, 10: H-fix, 11: normal
ANALOG_ON	0	0	DAC/PLL power ON/OFF setting for Audio 0: Power OFF 1: Power ON

※1 When HDMI Not used, and the HDMI Audio clock is stopped, this address is set to 10h. When using HDMI always set to 31h.

7.9.3.11 AVMUTE CONTROL (AVM_CTL) (0x8546)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVM_CTL							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
AVM_CTL	7:0	0	AVMUTE automatic clear setting After moving to AVMUTEm status, if the SET_AVMUTE/CLEAR_AVMUTE is not received, the allowed time is set. When the set allowed time is reached, AVMUTE status is automatically cleared. Allowed time = Setting value * 100msec If Setting value = 8'h00, automatic clear is not performed. 【Note】Valid for Video/Audio mute circuit only. HDCP state machine is reidentified and automatically cleared. If PHY-A/B switching, DDC5V=L, and DVI move has occurred, AVMUTE is cleared regardless of this register setting.

7.9.3.12 SOFTWARE RESET Register (SOFT_RST) (0x8547)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		SRST_SH	SRST_HP	SRST_I2CK	Reserved	SRST_I2CD	SRST_PI
Type	RO		RW	RW	RW	RO	RW	RW
Default	0		0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:6]	0	
SRST_SH	5	0	V' value calculation state machine reset 1: Reset (Auto clear)
SRST_HP	4	0	HDCP state machine reset 1: Reset (Auto clear)

SRST_I2CK	3	0	Key EEPROM I2C state machine reset 1: Reset (Auto clear)
Reserved	2	0	
SRST_I2CD	1	0	DDC I2C state machine reset, 1: Reset (Auto clear)
SRST_PI	0	0	TMDS decoder reset 1: Reset (Auto clear)

7.9.3.13 INIT END REGISTER (INIT_END) (0x854A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							INIT_END
Type	RO							RW
Default	0							0

Register Field	Bit	Default	Description
Reserved	7:1	0x0	
INIT_END	0	0x0	Initialization completed flag After completion of all initialization settings, write “1” to this register. If 0x8544[4] = 1, HPDO is asserted only when INIT_END is asserted. If 0x8543[2] = 1, DDC is active only when INIT_END is asserted

7.9.3.14 HDCP MODE Register (HDCP_MODE) (0x8560)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		Mode_RST_TN	Line_Rekey	Reserved	AUTO_CLR	Reserved	
Type	RO		RW	RW	RO	RW	RO	
Default	0		1	0	0	0	0	

Register Field	Bit	Default	Description
Reserved	[7:6]	0	
Mode_RST_TN	5	1	HDCP automatic reset when DVI⇔HDMI switched 0: Automatic reset OFF 1: Automatic reset ON
Line_Rekey	4	0	HDCP Line Rekey timing switch 0: 57clk mode (Data island delay ON)

			1: 58clk mode (Data island delay OFF)
Reserved	3	0	
AUTO_CLR	2	0	Bcaps[5] KSVINFO_READY(0x8840[5]) auto clear mode 0: No auto clear using AKSV write 1: Auto clear using AKSV write
Reserved	[1:0]	0	

7.9.3.15 HDCP COMMAND Register (HDCP_CMD) (0x8561)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				ShaS	Reserved		UnAuth
Type	RO				RW	RO		RW
Default	0x0				0	0x0		0

Register Field	Bit	Default	Description
Reserved	[7:4]	0	
ShaS	3	0	V' value calculation start command (After calculation completed, automatically clears) 1: Command issued
Reserved	[2:1]	0	
UnAuth	0	0	Unauthorized move command (automatic clear) 1: Command issued

7.9.3.16 VI MODE REGISTER (VI_MODE) (0x8570)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			SG_ON	Reserved			
Type	R/W			RW	R/W			
Default	1	1	1	0	1	1	1	0

Register Field	Bit	Default	Description
Reserved	7:5	0x7	Do not change reserved value
SG_ON	4	0x0	Input HSYNC jitter absorption control 0: Jitter absorption OFF 1: Jitter absorption ON Note: Removes HSYNC jitter of +/- 1clk or less, and corrects

			HSYNC phase shift of +/-4 clk or less
Reserved	3:0	0xE	Do not change reserved value

7.9.3.17 VOUT SET REGISTER (VOUT_SET) (0x8573)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Sel422	VOUT_422FIL			Reserved		VOutColorMode	
Type	RW	RW			R/W		R/W	
Default	1	0x0			0x0		0x0	

Register Field	Bit	Default	Description
Sel422	7	0x1	Video output 422/444 Selection 0: 444 fixed output 1: 422 fixed output
VOUT_422FIL	6:4	0x0	Video Output 422 conversion mode selection 000: Normally 2 tap filter 001: Normally 3 tap filter 010: Normally simple thinning 011: During 444 input, 2tap filter; during 422 input, simple thinning 100: During 444 input, 3tap filter; during 422 input, simple thinning 101: When 444 input or matrix ON, 3tap filter; Other is simple thinning 11x: When 444 input or matrix ON, 3tap filter; Other is simple thinning Note: When 444 fixed output is selected, automatically becomes 422 conversion OFF
Reserved	3:2	0x0	
VOutColorMode	1:0	0x0	VIDEO output Color mode setting 00: Through mode (Input is output as is) 01: Internal coefficient for automatic conversion mode (Fixed Color output) 10: xvYCC, sYCC, Adobe YCC601 are through, Adobe RGB is automatically converted to Adobe YCC601, All others are automatically converted by internal coefficient **(TBD: Recommendation by TSBJ is to not use this setting)** 11: HOST setting matrix coefficient (address0x85b0～c1) calculation mode

7.9.3.18 VOUT SET3 REGISTER (VOUT_SET3) (0x8574)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VOUT_LIM	Reserved	VOUT_BIT		VOUT_EXTCNT	Reserved		
Type	R/W	R/W	R/W		R/W	R/W		
Default	0	0	0		0	0		

Register Field	Bit	Default	Description
VOUT_LIM	7	0x0	Video output limiter On/Off setting 0: Limiter OFF 1: Limiter ON (all “0” and all “1” prohibited) Valid in all Y/G, Cb/B andCr/R
Reserved	6	0x0	
VOUT_BIT	5:4	0x0	Output bit rounding setting 00 : 16bit 01: 12bit (Rounded up) 10: 10bit (Rounded up) 11: 8bit (Rounded up)
VOUT_EXTCNT	3	0x0	444 / 422 output switching method 0 : Follow control from later stage block 1: Follow 0x8573 bit 7 setting
Reserved	2:0	0x0	

7.9.3.19 VOUT COLOR REGISTER (VI_REP) (0x8576)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VOUT_COLOR_SEL			IN_REP_HEN	IN_REP			
Type	RW			RW	R/W			
Default	0x03			0x0	0x0			

Register Field	Bit	Default	Description
VOUT_COLOR_SEL	7:5	0x3	Output Color setting 000: RGB Full 001: RGB Limited 010: 601YCbCr Full 011: 601 YCbCr Limited 100: 709 YCbCr Full

			101: 709 YCbCr Limited 110: Range conversion （Full→Limited) 111: Range conversion （Limited→Full) When VOUT_COLOR_MODE==00 (Through), this bit setting is invalid.
IN_REP_HEN	4	0x0	Input Pixel Repetition judgment Automatic/HOST setting switch 0: Automatic setting 1: HOST setting
IN_REP	3:0	0x0	Input Pixel Repetition HOST setting 0 : No Repetition 1: Repetition=2 2: Repetition=3 3: Repetition=4 …… 9: Repetition=10 10 ～15 : Setting prohibited

7.9.3.20 DC MODE REGISTER (DC_MODE) (0x8577)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DC_NOCD_NUN				Reserved			
Type	R/W				R/W			
Default	0x0				0x0			

Register Field	Bit	Default	Description
DC_NOCD_NUN	7:4	0x0	Threashold value for automatic move to 24bit mode when either GC packet input or GC Packet non-input have occurred in succession alongside DC_NOCD_SEL setting condition CD Sets above condition successive occurrence V number At 0000 setting, automati move OFF (default) Note: In the standard, setting 4 (0100) is recommended
Reserved	3:0	0x7	Do not change reserved value

7.9.3.21 EDID MODE REGISTER (EDID_MODE) (0x85C7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	EDID_SPEED			Reserved		EDID_MODE	
Type	RO	R/W			RO		R/W	
Default	0x0	0x0			0x0		0x0	

Register Field	Bit	Default	Description
Reserved	7	0x0	
EDID_SPEED	6:4	0x0	EDID dedicated terminal I2C speed selection 000: 100KHz 001: 400KHz
Reserved	3:2	0x0	
EDID_MODE	1:0	0x0	EDID access response mode selection 00: DDC line direct connection EEPROM mode (Absolutely no response to EDID access from DDC line) 01: Internal EDID-RAM & DDC2B mode (No response to 0x60slave =>Returns NACK) 1x: Internal EDID-RAM & E-DDC mode

7.9.3.22 EDID Slave REGISTER (EDID_SLV) (0x85C8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EDID_SLV							
Type	R/W							
Default	0xA0							

Register Field	Bit	Default	Description
EDID_SLV	7:0	0xA0	EDID EEPROM SLAVE address setting Note: Fixed at bit0=0

7.9.3.23 EDID Offset REGISTER (EDID_OFF) (0x85C9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EDID_OFF							
Type	R/W							
Default	0x00							

Register Field	Bit	Default	Description
EDID_OFF	7:0	0x00	EDID EEPROM Read start offset address setting

7.9.3.24 EDID Length REGISTER 1 (EDID_LEN1) (0x85CA)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EDID_LEN[7:0]							

Type	R/W
Default	0x00

Register Field	Bit	Default	Description
EDID_LEN[7:0]	7:0	0x00	EDID data size stored in RAM Note: Sets Data byte number Read from EEPROM Note: If EDID_LEN[10:0]=0 is set, no read Note: if EDID_LEN[10:0]>0x400 (1024 or more) is set, 1024 bytes only are Read Note: If EEPROM not used, and data is written directly to RAM from HOST, data size is set

7.9.3.25 EDID Length REGISTER 2 (EDID_LEN2) (0x85CB)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					EDID_LEN[10:8]		
Type	RO					R/W		
Default	0x00					0x0		

Register Field	Bit	Default	Description
Reserved	7:3	0x00	Reserved
EDID_LEN[10:8]	2;0	0x0	EDID data size stored in RAM (upper address bits)

7.9.3.26 EDID Command REGISTER (EDID_CMD) (0x85CC)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						ED_RST_CMD	ED_CMD
Type	RO						R/W	R/W
Default	0x00						0x0	0x0

Register Field	Bit	Default	Description
Reserved	7:2	0x00	Reserved
ED_RST_CMD	1	0x0	EDID EEPROM reset operation start command 1: Command issued Note: After reset action ended, automatically clears to “0”
ED_RD_CMD	0	0x0	Data forwarded to EDID-RAM from EEPROM start command 1: Command issues

			Note: After reset action ended, automatically clears to “0”

7.9.4 HDMI Rx Audio Control

7.9.4.1 FORCE MUTE (FORCE_MUTE) (0x8600)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			FORCE_AMUTE	Reserved			FORCE_DMUTE
Type	RO			RW	RO			RW
Default	0	0	0	1	0	0	0	1

Register Field	Bit	Default	Description
FORCE_AMUTE	4	0x1	Forced AMUTEOUT terminal control 0： Mute OFF, 1： Mute ON 【Note】 Setting and clear is possible at HOST only 【Note】 For Mute ON polarity, follow the 0x8608[5] setting
FORCE_DMUTE	0	0x1	Forced data MUTE control 0： Mute OFF, 1： Mute ON 【Note】 Setting and clear is possible at HOST only 【Note】 For Mute signal, follow the 0x8608[2:0] setting

7.9.4.2 CMD AUD (CMD_AUD) (0x8601)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					CMD_BUFINIT	CMD_LOCKDET	CMD_MUTE
Type	RO					RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
CMD_BUFINIT	2	0	Buffer initialization start command 0: Reset value 1: Command issued After buffer initialization completed, automatically clears When in automatic command issue mode (0x8604[2:1]≠2’b00), issue of commands from HOST is prohibited. When issuing commands from HOST, always issue the MUTE start command first.

CMD_LOCKDET	1	0	Audio clock frequency lock detection start command 0: Reset value 1: Command issued The reproduced Audio clock frequency detects unification with F_S information transmitted by Channel Status bit, and issues interrupt. For observation cycle and detection precision, follow the address 0x8630～33 setting. After frequency lock detection, automatically clears
CMD_MUTE	0	0	MUTE start command 0: Reset value 1: Command issued Automatic command issue mode exists. For automatic issue condition, follow the AUTO_CMD0, 1(address0x8602, 0x8603) setting. When AUTO_PLAY3 setting ON, automatically clears to "0" when Buffer initialization completed. For Mute signal, follow the 0x8608[2:0] setting For AMUTE terminal output polarity, follow the 0x8608[5] setting

7.9.4.3 Auto Command REGISTER 0 (AUTO_CMD0) (0x8602)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Auto_ Mute7	Auto_ Mute6	Auto_ Mute5	Auto_ Mute4	Auto_ Mute3	Auto_ Mute2	Auto_ Mute1	Auto_ Mute0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Auto_Mute7	7	In PHY-A/B switch, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute6	6	In LPCM/NLPCM change detection, automatically set CMD_MUTE 0: Not set, 1: Set OR conditions for LPCM → NLPCM detect and NLPCM → LPCM detect
Auto_Mute5	5	In F_S change detection, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute4	4	In PHY output clock change detection, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute3	3	In Non LPCM detection period, automatically set CMD_MUTE 0: Not set, 1: Set

Auto_Mute2	2	In Audio clock frequency unlock detect period, automatically set CMD_MUTE 0: Not set, 1: Set (**Use not recommended**)
Auto_Mute1	1	In PHY no output clock detect period, automatically set CMD_MUTE 0: Not set, 1: Set
Auto_Mute0	0	In DVI mode period, or in DDC5V =0V period, automatically set CMD_MUTE 0: Not set, 1: Set

7.9.4.4 Auto Command REGISTER 0 (AUTO_CMD1) (0x8603)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					Auto_Mute10	Auto_Mute9	Auto_Mute8
Type	RO					RW	RW	RW
Default	0x00					0	0	0

Register Field	Bit	Description
Reserved	[7:3]	
Auto_Mute10	2	In 60958 frame discontinuous detect, automatically issue CMD_MUTE 0: Not issue, 1: Issue
Auto_Mute9	1	In SET_AVMUTE receive period, automatically issue CMD_MUTE 0: Not issue, 1: Issue
Auto_Mute8	0	In buffer flow detect, automatically issue CMD_MUTE 0: Not issue, 1: Issue

7.9.4.5 Auto Command REGISTER 0 (AUTO_CMD2) (0x8604)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				Auto_Play3	Auto_Play2	Reserved	
Type	RO				RW	RW	RO	
Default	0x0				0	0	0x0	

Register Field	Bit	Description
Reserved	[7:4]	
Auto_Play3	3	In Buffer initialization end detect, automatically clears MUTE_CMD 0: Not clear, 1: Clear

Auto_Play2	2	After generation of MUTE factor selected in AUTO_MUTE setting "after fixed time B" automatically issue CMD_BUFINIT 0: Not issue, 1: Issue Priority over frequency lock detect (=equivalent to lock detect time limit) If MUTE factor continues for fixed period, issue command at end edge of factor. If MUTE factor is generated during fixed time measurement, restart time measurement from beginning.
Reserved	[1:0]	

7.9.4.6 Buffer Initialization Start Period (BUFINIT_START) (0x8606)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	BUFINIT_START							
Type	RW							
Default	0x0A							

Register Field	Bit	Description
BUFINIT_START	[7:0]	Wait time setting until Buffer initialization start in AUTO_PLAY2 → "fixed time B" 0.1 ～ 25.5sec. (set in 0.1 sec. units) Setting of 0 sec. (00h) is prohibited

7.9.4.7 FS MUTE REGISTER (FS_MUTE) (0x8607)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	FS_else_MUTE	FS22_MUTE	FS24_MUTE	FS88_MUTE	FS96_MUTE	FS176_MUTE	FS192_MUTE	FS_NO_MUTE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
FS_else_MUTE	7	0x1	Other than F_S = 22k,24k,32k,44k,48k,88k,96,176k,192k 0 : Do not Mute, 1 : Mute
FS22_MUTE	6	0x1	When at F_S = 22.05KHz, routinely 0 : Do not Mute, 1 : Mute

FS24_MUTE	5	0x1	When at F_S = 24KHz, routinely 0 : Do not Mute, 1 : Mute
FS88_MUTE	4	0x1	When at F_S = 88.2KHz, routinely 0 : Do not Mute, 1 : Mute
FS96_MUTE	3	0x1	When at F_S = 96KHz, routinely 0 : Do not Mute, 1 : Mute
FS176_MUTE	2	0x1	When at F_S = 176.4KHz, routinely 0 : Do not Mute, 1 : Mute
FS192_MUTE	1	0x1	When at F_S = 192KHz, routinely 0 : Do not Mute, 1 : Mute
FS_NO_MUTE	0	0x1	When at F_S = not indicated, routinely 0 : Do not Mute, 1 : Mute

Write FS Bit corresponding to set specification to ”0”.
F_S =48KHz, 44.1KHz, 32KHz are outside FS_MUTE applicability. (In the standard, 48KHz, 44.1KHz, 32KHz must be reproduced)

7.9.4.8 AUDIO SAMPLE FREQUENCY INPUT MODE (FS_IMODE) (0x8620)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	NLPCM_ HMODE	NLPCM_ SMODE	NLPCM_ IMODE	FS_ HMODE	FS_ AMODE	FS_ SMODE	FS_ IMODE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	7	
NLPCM_HMODE	6	LPCM/NLPCM identification information HOST setting mode 0 : OFF (=automatic setting) 1 : At HOST only, set identification information to 0x8621[4]
NLPCM_SMODE	5	LPCM/NLPCM identification information extraction mode setting 0 : Information extracted from C_bit only 1 : Information extracted at AUD_Info priority
NLPCM_IMODE	4	Action setting during CBIT- NLPCM bit error 0 : When subpacket error includes the bit, update not performed 1 : When subpacket error includes the bit, update performed
FS_HMODE	3	F_S (sampling frequency) HOST setting mode 0 : OFF (=automatic setting) 1 : At HOST only, set F_S information to 0x8621[3:0]

FS_AMODE	2	Sampling frequency due to ACR (N/CTS value) automatic calculation mode setting 0 : OFF 1 : Calculation result at highest priority
FS_SMODE	1	F_S (sampling frequency) identification information extraction mode setting 0 : Information extracted from C_bit only 1 : Information extracted at AUD_Info priority
FS_IMODE	0	Action setting during CBIT-FS bit error 0 : When subpacket error includes the bit, update not performed 1 : When subpacket error includes the bit, update performed

7.9.4.9 AUDIO SAMPLE FREQUENCY MODE REGISTER (FS_SET) (0x8621)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DTS Double	Reserved		NLPCM	FS			
Type	RW	RW		RW	RW			
Default	0	0		0	0x2			

Register Field	Bit	Description
DTS Double	7	DST double rate flag monitor (When other than DST selected, fixed at 0) 0: normal rate, 1: double rate
Reserved	[6:5]	
NLPCM	4	Normal Audio linear PCM/nonlinear PCM identification information extraction result 0: LPCM 1: Compression stream [Note] When 0x8620[6]==0, Follow the 0x8620[5:4] setting, and HW automatically set, write from Host is invalid. If 0x0620[6]==1, HOST determines and sets. [Note]LPCM/NLPCM change interrupt (address0x8505[3:2]) is generated when this register has a change.
FS	[3:0]	AUDIO sampling frequency information extraction result 4'h0: 44.1KHz, 4'h2: 48KHz, 4'h3: 32KHz, 4'h4: 22.05KHz, 4'h6: 24KHz, 4'h8: 88.2KHz, 4'hA: 96KHz, 4'hC: 176.4KHz, 4'hE: 192KHz, **4'h9: 768KHz** **4'h5: 384KHz, 4'h7: 352.8KHz, 4'hB: 705.6KHz** [Note]

		If 0x08620[3]==0, Follow 0x8620[2:0] setting, HW is automatically set, write from Host is invalid. If 0x8620[3]==1, Host determines and sets. [Note] F_S change interrupt (address0x08505[1]) is generated when this register has a change.

7.9.4.10 Audio FS Lock Detect Control REGISTER 0 (LKDet_REF0) (0x8630)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LOCK_REF[7:0]							
Type	RW							
Default	0xA0							

Register Field	Bit	Description
LOCK_REF[7:0]	[7:0]	RefClk cycle number setting during 10msec 20 bit Initial value = 420000= 668A0h (for 42MHz) = 270000 = 41EB0h (for 42MHz)

7.9.4.11 Audio FS Lock Detect Control REGISTER 1 (LKDet_REF1) (0x8631)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LOCK_REF[15:8]							
Type	RW							
Default	0x68							

Register Field	Bit	Description
LOCK_REF[15:8]	[7:0]	RefClk cycle number setting during 10msec 20 bit Initial value = 420000= 668A0h (for 42MHz) = 270000 = 41EB0h (for 42MHz)

7.9.4.12 Audio FS Lock Detect Control REGISTER 0 (LKDet_REF2) (0x8632)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				LOCK_REF[19:16]			
Type	RO				RW			
Default	0x0				0x6			

Register Field	Bit	Description
Reserved	[7:4]	
LOCK_REF[19:16]	[3:0]	RefClk cycle number setting during 10msec 20 bit Initial value = 420000= 668A0h (for 42MHz) = 270000 = 41EB0h (for 42MHz)

7.9.4.13 CTS Adjustment Mode REGISTER 1 (ACR_MODE) (0x8640)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			ACR_LOAD	Reserved	N_MODE	CTS_MODE	
Type	RO			RW	RO	RW	RW	
Default	0x0			0	0	0	2'b0	

Register Field	Bit	Description
Reserved	[7:5]	
ACR_LOAD	4	N/CTS value forced load command 0: Normal action 1: Command issued 【Note】Automatic clear
Reserved	3	Reserved
N_MODE	2	Audio PLL N value update action setting 0: Uses receive N value (normal action) 1: Uses HOST setting N value (for test)
CTS_MODE	[1:0]	Audio PLL CTS value update action setting 00: Uses receive CTS value (normal action) 01: Uses HW correction CTS value (HW automatic flow control) 【Note】 In HW automatic flow control mode, the received CTS is corrected and PLL applied, in response to Audio Buffer balance state. When this function is used, even if illegitimate (violation of standard) CTS is received, undestroyed Audio replay is possible. The CTS correction amount is set at address 0x8641～0x8642.

7.9.4.14 CTS Adjustment REGISTER 0 (ACR_MDF0) (0x8641)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	ACR_L2MDF			Reserved	ACR_L1MDF		
Type	RO	RW			RO	RW		

Default	0	3'b010	0	3'b001

Register Field	Bit	Description
Reserved	7	
ACR_L2MDF	[6:4]	CTS correction amount setting with Buffer linear Over/Under (Threshold 2) detection 000: ±0ppm (±0) 001: ±61ppm (±1/16384*CTS) 010: ±122ppm (±1/8192*CTS) 011: ±244ppm (±1/4096*CTS) 100: ±488ppm (±1/2048*CTS) 101: ±976ppm (±1/1024*CTS) 110: ±1976ppm (±1/512*CTS) 111: ±3906ppm (±1/256*CTS)
Reserved	3	Reserved
ACR_L1MDF	[2:0]	CTS correction amount setting with Buffer linear Over/Under (Threshold 1) detection 000: ±0ppm (±0) 001: ±61ppm (±1/16384*CTS) 010: ±122ppm (±1/8192*CTS) 011: ±244ppm (±1/4096*CTS) 100: ±488ppm (±1/2048*CTS) 101: ±976ppm (±1/1024*CTS) 110: ±1976ppm (±1/512*CTS) 111: ±3906ppm (±1/256*CTS)

7.9.4.15 CTS Adjustment REGISTER 0 (ACR_MDF1) (0x8642)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					ACR_L3MDF		
Type	RO					RW		
Default	0x00					3'b011		

Register Field	Bit	Description
Reserved	[7:3]	Reserved
ACR_L3MDF	[2:0]	CTS correction amount setting with Buffer Over/Undr detection 【Note】If Over/Under flow prevention control OFF, set to ±0ppm

		000: ±0ppm (±0) 001: ±61ppm (±1/16384*CTS) 010: ±122ppm (±1/8192*CTS) 011: ±244ppm (±1/4096*CTS) 100: ±488ppm (±1/2048*CTS) 101: ±976ppm (±1/1024*CTS) 110: ±1976ppm (±1/512*CTS) 111: ±3906ppm (±1/256*CTS)

7.9.4.16 AUDIO OUTPUT MODE 0 Register (SDO_MODE0) (0x8651)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIT_CBIT	DIT_BIT_LEN	SPDIF_EN	Reserved	BCK_POL	BCK_FS	LR_POL
Type	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Default	Description
Reserved	7		Reserved
DIT_CBIT	6	0	SPDIF output C-bit superposition method selection 0: Not through Audio Buffer. User-bit is not superposed. 1: Through Audio Buffer. User-bit is superposed, but if Buffer flow is generated, both C-bit & User-bit are destroyed.
DIT_BIT_LEN	5	0	SPDIF output bit length selection 0: Original Bit length 1: 16-bit limit (lower 8-bit discarded)
SPDIF_EN	4	0	SPDIF Format Enable 0: Serial format audio data output (same as I2S channels 0-2) 1: SPDIF (60958) Format on I2S output pin3
Reserved	3		Reserved
BCK_POL	2	0	BCK polarity selection 0: Normal (Data changed on falling edge) 1: Inverted (Data changed on rising edge)
BCK_FS	1	1	BCK frequency selection 0: 32 Fs 1: 64 Fs
LR_POL	0	0	LRCK polarity selection 0: Normal (sample period: 1st half=L, 2nd half = H) 1: Inverted (sample period: 1st half = H, 2nd half = L)

7.9.4.17 AUDIO OUTPUT MODE 1 Register (SDO_MODE1) (0x8652)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	SDO_BIT_LENG			I2S_HBR4L_MODE	I2S_MODE	SDO_FMT	
Type	RO	R/W			R/W	R/W	R/W	
Default	0	3'b110			1'b0	1'b0	2'b00	

Register Field	Bit	Default	Description
	7	0	Reserved
SDO_BIT_LENG	6:4	3'b110	ASDO output data Bit Length setting 000: 16bit (lower 8bit discarded) 001: 16bit (lower 8bit + 1 discarded) 010: 18bit (lower 6bit discarded) 011: 18bit (lower 6bit + 1 discarded) 100: 20bit (lower 4bit discarded) 101: 20bit (lower 4bit + 1 discarded) 110: 24bit no rounding 111: Output OFF (Mute)
I2S_HBR4L_MODE	3	1'b0	I2S HBR 4-Lane Mode 1: HBR 4-Lane mode 0: HBR 1-Lane mode
I2S_MODE	2	1'b0	I2S Mode 1: I2S with BCUVP 0: Normal (I2S/Left-J/Right-J)
SDO_FMT	1:0	2'b00	ASDO output format setting 00: Right justified 01: Left justified 1x: I2S

7.9.4.18 AUDIO OUTPUT CHAN_SEL 3 Register (SDO_CHSEL3) (0x8656)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SDO3R_ASSIGN				SDO3L_ASSIGN			
Type	R/W				R/W			
Default	0x8				0x7			

Register Field	Bit	Default	Description
SDO3R_ASSIGN	7:4	0x8	SPDIF output channel setting 0000: Output OFF (=MUTE)

			0001: CH1 0010: CH2 0011: CH3 0100: CH4 0101: CH5 0110: CH6 0111: CH7 1000: CH8 Other: CH8
SDO3L_ASSIGN	3:0	0x7	SPDIF output channel setting 0000: Output OFF (=MUTE) 0001: CH1 0010: CH2 0011: CH3 0100: CH4 0101: CH5 0110: CH6 0111: CH7 1000: CH8 Other: CH7

7.9.4.19 AUDIO DIV Mode Register (DIV_MODE) (0x8665)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DIV_DLY				Reserved			DIV_MODE
Type	R/W				RO			R/W
Default	0x0				0x0			0x0

Register Field	Bit	Default	Description
DIV_DLY	7:4	0x0	Divider switch timing setting for AMCK, CLK128FS generation After FS change interrupt is generated, delay until Audio clock frequency is actually switched is set in 0.1 sec. units (No delay at 4'b0000 setting)
Reserved	3:1	0x0	
DIV_MODE	0	0x0	Division ratio of divider for AMCK, CLK128FS generation, and F0 selection (44.1 series, 48 series) setting mode 0: Automatic setting 1: HOST setting

7.9.4.20 AUDIO DIV CLK Register (DIV_CLK) (0x8666)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	F0_SEL	DIV_AMCK			DIV_128FS			
Type	R/W	R/W			R/W			
Default	0x0	0x1			0x5			

Register Field	Bit	Default	Description
F0_SEL	7	0x0	VCO oscillation frequency (F0) setting 0: 48KHz series (0x2572FB0) --- VCO output= 98.304MHz 1: 44KHz series (0x22680A0) --- VCO output= 90.3168MHz During automatic setting mode, HW automatically writes to this register
DIV_AMCK	6:4	0x1	Division setting value during AMCK generation 000 = 1/2, 001=1/4(Initial value), 010=1/6, 011=1/8, 100 = 1/12, 101=1/16, 110=1/24, 111= thru (1/1) During automatic setting mode, HW automatically writes to this register However, division value for each FS is set anew by the HOST. HW is only selected using FS information.
DIV_128FS	3:0	0x5	Division setting value for CLK128FS generation 0000 = 1/2, 0001=1/4, 0010=1/6, 0011=1/8, 0100 = 1/12, 0101=1/16(Initial value), 0110=1/24, 0111=1/32, 1xxx = thru (1/1) During automatic setting mode, HW automatically writes to this register However, division value for each FS is set anew by the HOST. HW is only selected using FS information.

7.9.4.21 AUDIO DIV24 SEL Register (DIV24_SEL) (0x8667)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIV_24K_AMCK			DIV_24K_128F			
Type	RO	R/W			R/W			
Default	0x0	0x5			0x7			

Register Field	Bit	Default	Description
Reserved	7	0x0	
DIV_24K_AMCK	6:4	0x5	Division setting for AMCK generation when FS=24KHz or 22.05KHz 000 = 1/2, 001=1/4, 010=1/6, 011=1/8, 100 = 1/12, 101=1/16 (Initial value), 110=1/24, 111= thru (1/1)
DIV_24K_128F	3:0	0x7	Division setting for 128FS generation when FS=24KHz or

			22.05KHz 0000 = 1/2, 0001=1/4, 0010=1/6, 0011=1/8, 0100 = 1/12, 0101=1/16, 0110=1/24, 0111=1/32 (Initial value), 1xxx = thru (1/1)

7.9.4.22 AUDIO DIV32 SEL Register (DIV32_SEL) (0x8668)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIV_32K_AMCK			DIV_32K_128F			
Type	RO	R/W			R/W			
Default	0x0	0x5			0x7			

Register Field	Bit	Default	Description
Reserved	7	0x0	
DIV_32K_AMCK	6:4	0x5	Division setting for AMCK generation when FS=32KHz 000 = 1/2, 001=1/4, 010=1/6, 011=1/8, 100 = 1/12, 101=1/16 (Initial value), 110=1/24, 111= thru (1/1)
DIV_32K_128F	3:0	0x7	Division setting for 128FS generation when FS=32KHz 0000 = 1/2, 0001=1/4, 0010=1/6, 0011=1/8, 0100 = 1/12, 0101=1/16, 0110=1/24, 0111=1/32 (Initial value), 1xxx = thru (1/1)

7.9.4.23 AUDIO DIV48 SEL Register (DIV48_SEL) (0x8669)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIV_48K_AMCK			DIV_48K_128F			
Type	RO	R/W			R/W			
Default	0x0	0x3			0x5			

Register Field	Bit	Default	Description
Reserved	7	0x0	
DIV_48K_AMCK	6:4	0x3	Division setting for AMCK generation when FS=48KHz or 44.1KHz 000 = 1/2, 001=1/4, 010=1/6, 011=1/8 (Initial value), 100 = 1/12, 101=1/16, 110=1/24, 111= thru (1/1)
DIV_48K_128F	3:0	0x5	Division setting for 128FS generation when FS=48KHz or 44.1KHz 0000 = 1/2, 0001=1/4, 0010=1/6, 0011=1/8, 0100 = 1/12, 0101=1/16 (Initial value), 0110=1/24,

			0111=1/32, 1xxx = thru (1/1)

7.9.4.24 AUDIO DIV96 SEL Register (DIV96_SEL) (0x866A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIV_96K_AMCK			DIV_96K_128F			
Type	RO	R/W			R/W			
Default	0x0	0x1			0x3			

Register Field	Bit	Default	Description
Reserved	7	0x0	
DIV_96K_AMCK	6:4	0x1	Division setting for AMCK generation when FS=96KHz or 88.2KHz 000 = 1/2, 001=1/4 (Initial value), 010=1/6, 011=1/8, 100 = 1/12, 101=1/16, 110=1/24, 111= thru (1/1)
DIV_96K_128F	3:0	0x3	Division setting for 128FS generation when FS=96KHz or 88.2KHz 0000 = 1/2, 0001=1/4, 0010=1/6, 0011=1/8 (Initial value), 0100 = 1/12, 0101=1/16, 0110=1/24, 0111=1/32, 1xxx = thru (1/1)

7.9.4.25 AUDIO DIV192 SEL Register (DIV192_SEL) (0x866B)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIV_192K_AMCK			DIV_192K_128F			
Type	RO	R/W			R/W			
Default	0x0	0x1			0x1			

Register Field	Bit	Default	Description
Reserved	7	0x0	
DIV_192K_AMCK	6:4	0x1	Division setting for AMCK generation when FS=192KHz or 176.4KHz 000 = 1/2, 001=1/4 (Initial value), 010=1/6, 011=1/8, 100 = 1/12, 101=1/16, 110=1/24, 111= thru (1/1)
DIV_192K_128F	3:0	0x1	Division setting for 128FS generation when FS=192KHz or 176.4KHz 0000 = 1/2, 0001=1/4 (Initial value), 0010=1/6, 0011=1/8, 0100 = 1/12, 0101=1/16, 0110=1/24, 0111=1/32,

			1xxx = thru (1/1)

7.9.4.26 AUDIO DIV768 SEL Register (DIV768_SEL) (0x866C)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIV_768K_AMCK			DIV_768K_128F			
Type	RO	R/W			R/W			
Default	0x0	0x7			0x8			

Register Field	Bit	Default	Description
Reserved	7	0x0	
DIV_768K_AMCK	6:4	0x7	Division setting for AMCK generation when FS=768KHz or 705.6KHz 000 = 1/2, 001=1/4, 010=1/6, 011=1/8, 100 = 1/12, 101=1/16, 110=1/24, 111= thru (1/1) (Initial value)
DIV_768K_128F	3:0	0x8	Division setting for 128FS generation when FS=768KHz or 705.6KHz 0000 = 1/2, 0001=1/4, 0010=1/6, 0011=1/8, 0100 = 1/12, 0101=1/16, 0110=1/24, 0111=1/32, 1xxx = thru (1/1) (Initial value)

7.9.4.27 AUDIO DIV384 SEL Register (DIV384_SEL) (0x866D)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	DIV_384K_AMCK			DIV_384K_128F			
Type	RO	R/W			R/W			
Default	0x0	0x0			0x0			

Register Field	Bit	Default	Description
Reserved	7	0x0	
DIV_384K_AMCK	6:4	0x0	Division setting for AMCK generation when FS=384KHz or 352.8KHz 000 = 1/2 (Initial value), 001=1/4, 010=1/6, 011=1/8, 100 = 1/12, 101=1/16, 110=1/24, 111= thru (1/1)
DIV_384K_128F	3:0	0x0	Division setting for 128FS generation when FS=384KHz or 352.8KHz 0000 = 1/2 (Initial value), 0001=1/4, 0010=1/6, 0011=1/8, 0100 = 1/12, 0101=1/16, 0110=1/24, 0111=1/32,

			1xxx = thru (1/1)

7.9.4.28 AUDIO PLL Setting Register (NCO_F0_MOD) (0x8670)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						NCO_F0_MOD	
Type	RO						R/W	
Default	0x0						2'b00	

Register Field	Bit	Default	Description
Reserved	7:2	0x0	
NCO_F0_MOD	1:0	0x0	NCO standard frequency setting for Audio PLL 00: For REFCLK = 42MHz 01: For REFCLK = 27MHz 1x: Reserved

7.9.4.29 AUDIO PLL Setting Register (NCO_48F0A) (0x8671)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[7:0]							
Type	RW							
Default	0x00							

7.9.4.30 AUDIO PLL Setting Register (NCO_48F0B) (0x8672)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[15:8]							
Type	RW							
Default	0x00							

7.9.4.31 AUDIO PLL Setting Register (NCO_48F0C) (0x8673)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[23:16]							
Type	RW							
Default	0x00							

7.9.4.32 AUDIO PLL Setting Register (NCO_48F0D) (0x8674)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				NCO_48F0[27:24]			
Type	RO				RW			
Default	0x0				0x0			

7.9.4.33 AUDIO PLL Setting Register (NCO_44F0A) (0x8675)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_44F0[7:0]							
Type	RW							
Default	0x00							

7.9.4.34 AUDIO PLL Setting Register (NCO_44F0B) (0x8676)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_44F0[15:8]							
Type	RW							
Default	0x00							

7.9.4.35 AUDIO PLL Setting Register (NCO_44F0C) (0x8677)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_44F0[23:16]							
Type	RW							
Default	0x00							

7.9.4.36 AUDIO PLL Setting Register (NCO_44F0D) (0x8678)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				NCO_44F0[27:24]			
Type	RO				RW			
Default	0x0				0x0			

7.9.4.37 AUDIO DSD Mode Register (EX_MODE) (0x8680)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						EX_AUDIO	
Type	RO						RW	
Default	0x0						0x0	

Register Field	Bit	Default	Description
EX_AUDIO	1:0	0x0	AUDIO replay packet selection 00: Normal Audio (packet type = 0x02) 01: HBR Audio (packet type = 0x09) 10: Reserved 11: Reserved Whenever HBR audio detection is enabled from EX_AUDIO_MODE , user has to program 16'h8601 CMD_MUTE to clear mute and CMD_BUFINIT =1

7.9.4.38 AUDIO OUTPUT MODULE TERMINAL CONTROL (APIN_EN0) (0x8690)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AMTSEL		ALRSEL		ABCKSEL		AMCKSEL	
Type	RW		RW		RW		RW	
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
AMTSEL	7:6	0x3	AMUTE (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal
ALRSEL	5:4	0x3	LRCK (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal
ABCKSEL	3:2	0x3	BMCK (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal
AMCKSEL	1:0	0x3	AMCK (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal

7.9.5 HDMI Rx InfoFrame Data

7.9.5.1 VS INFO PACKET TYPE CODE SETTING (TYP_VS_SET) (0x8701)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_VS_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_VS_SET	7:0	X	VS_info Packet Type code setting

7.9.5.2 AVI INFO PACKET TYPE CODE SETTING (TYP_AVI_SET) (0x8702)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_AVI_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_AVI_SET	7:0	X	AVI_info Packet Type code setting

7.9.5.3 SPD INFO PACKET TYPE CODE SETTING (TYP_SPD_SET) (0x8703)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_SPD_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_SPD_SET	7:0	X	SPD_info Packet Type code setting

7.9.5.4 AUD INFO PACKET TYPE CODE SETTING (TYP_AUD_SET) (0x8704)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_AUD_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_AUD_SET	7:0	X	AUD_info Packet Type code setting

7.9.5.5 MS INFO PACKET TYPE CODE SETTING (TYP_MS_SET) (0x8705)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_MS_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_MS_SET	7:0	X	MS_info Packet Type code setting

7.9.5.6 ACP INFO PACKET TYPE CODE SETTING (TYP_ACP_SET) (0x8706)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ACP_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ACP_SET	7:0	X	ACP Packet Type code setting

7.9.5.7 ISRC1 INFO PACKET TYPE CODE SET. (TYP_ISRC1_SET) (0x8707)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ISRC1_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ISRC1_SET	7:0	X	ISRC1 Packet Type code setting

7.9.5.8 ISRC2 INFO PACKET TYPE CODE SETTING (TYP_ISRC2_SET) (0X8708)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ISRC2_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ISRC2_SET	7:0	X	ISRC2 Packet Type code setting

7.9.5.9 PACKET INTERRUPT MODE (PK_INT_MODE) (0x8709)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_INT_MODE	ISRC_INT_MODE	ACP_INT_MODE	VS_INT_MODE	SPD_INT_MODE	MS_INT_MODE	AUD_INT_MODE	AVI_INT_MODE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
ISRC2_INT_MODE	7	0	Action setting during ISRC2_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
ISRC_INT_MODE	6	0	Action setting during ISRC 1 packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
ACP_INT_MODE	5	0	Action setting during ACP packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
VS_INT_MODE	4	0	Action setting during VS_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
SPD_INT_MODE	3	0	Action setting during SPD_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
MS_INT_MODE	2	0	Action setting during MS_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
AUD_INT_MODE	1	0	Action setting during AUD_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST

AVI_INT_MODE	0	0	Action setting during AVI_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST

7.9.5.10 PACKET AUTO CLEAR (PK_AUTO_CLR) (0x870a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PK_AUTO_CLR7	PK_AUTO_CLR6	PK_AUTO_CLR5	PK_AUTO_CLR4	PK_AUTO_CLR3	PK_AUTO_CLR2	PK_AUTO_CLR1	PK_AUTO_CLR0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
PK_AUTO_CLR7	7	0	When DVI received, ISRC2_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR6	6	0	When DVI received, ISRC packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR5	5	0	When DVI received, ACP packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR4	4	0	When DVI received, VS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR3	3	0	When DVI received, SPD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR2	2	0	When DVI received, MS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR1	1	0	When DVI received, AUD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR0	0	0	When DVI received, AVI_info packet data cleared 1: Clear 0: Do not clear

7.9.5.11 NO PACKET LIMIT (NO_PK_LIMIT) (0x870b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NO_ACP_LIMIT				NO_AVI_LIMIT			
Type	RW	RW	RW	RW	RW	RW	RW	RW

Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_ACP_LIMIT	7:4	0	After receiving ACP packet, when ACP packet not received during settingvalue*80msec period, ACP receive interrupt occurs. 【Note】 At 4'b0000 setting, interrupt does not occur. 【Note】 At 4'b0000 setting, ACP packet receive status action does notoccur. 【Note】 When DVI received, interrupt does not occur.
NO_AVI_LIMIT	3:0	0	When AVI packet not received during setting value*80msec period, AVI receive interrupt occurs. 【Note】 At 4'b0000 setting, interrupt does not occur. 【Note】 When DVI received, interrupt does not occur.

7.9.5.12 NO PACKET CLEAR (NO_PK _CLR) (0x870c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	NO_VS_CLR	NO_SPD_CLR	NO_ACP_CLR	Reserved		NO_AVI_CLR1	NO_AVI_CLR0
Type	RW	RW	RW	RW	RO		RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_VS_CLR	6	0	When VS receive interrupt is detected, VS storage register automaticclear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_SPD_CLR	5	0	When SPD receive interrupt is detected, SPD storage registeautomatic clear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_ACP_CLR	4	0	When ACP receive interrupt is detected, ACP storage register automatic clear 1: Clear 0: Do not clear
NO_AVI_CLR1	1	0	When AVI receive interrupt occurs, judge input video signal with RGB and no Repetition 1: Judge 0: No judge (preserve in status before interruption)

NO_AVI_CLR0	0	0	When AVI receive interrupt is detected, AVI storage register automatic clear 1: Clear 0: Do not clear

7.9.5.13 ERROR PACKET LIMIT (ERR_PK_LIMIT) (0x870d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ERR_PK_MOD	ERR_PK_LIMIT						
Type	RW	RW						
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
ERR_PK_MOD	7	0x1	Packet continuing receive error detection start conditions 0: If error is included in either header/data 1: If correctable error was included in header
ERR_PK_LIMIT	6:0	0x7f	Packet continuing receive error occurrence detection threshold If error packet is continually received up to set Packet number value, Set Packet receive error status to “1”. If absolutely no error Packet is received, return Packet receive error status for both header/data to “0”. In 0 setting, detection OFF

7.9.5.14 NO PACKET LIMIT (NO_PK_LIMIT2) (0x870e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NO_VS_LIMIT				NO_SPD_LIMIT			
Type	RW				RW			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_VS_LIMIT	7:4	0	If no VS packet is received during setting value*80msec periodjudge receive interrupt has occurred. At 0000 setting, receivinterrupt detect is OFF.
NO_SPD_LIMIT	3:0	0	If no SPD packet is received during setting value*80msec periodjudge receive interrupt has occurred. At 0000 setting,

			receiveinterrupt detect is OFF.

7.9.5.15 VS IEEE SELECT (VS_IEEE_SEL) (0x870f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							VS_IEEE_SEL
Type	RO							RW
Default	0	0	0	0	0	0	0	1

Register Field	Bit	Default	Description
VS_IEEE_SEL	0	0x1	Extraction operation selection for VS Info packet stored at HDMI_VSInfo receive register (address0x8770～8e). 1: Store only when IEEE Registration Identifier is 0x000C03 VS_Infopacket only. 0: Freely store VS_Info packet regardless of IEEE Registration Identifier. 【Note】 This register setting is valid only at address0x8701[7:0]=81h. When address0x8701[7:0]≠81h, this register setting is ignored, and thespecified Type Packet is stored at address0x8770～8e each time it is received.

7.9.5.16 AVI INFO PACKET HEADER BYTE 0 (PK_AVI_0HEAD) (0x8710)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_0HEAD	7:0	X	861B AVI_info packet Header byte 0 (= type)

7.9.5.17 AVI INFO PACKET HEADER BYTE 1 (PK_AVI_1HEAD) (0x8711)

Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	AVI_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_1HEAD	7:0	X	861B AVI_info packet Header byte 1 (= version)

7.9.5.18 AVI INFO PACKET HEADER BYTE 2 (PK_AVI_2HEAD) (0x8712)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_2HEAD	7:0	X	861B AVI_info packet Header byte 2 (= data length)

7.9.5.19 AVI INFO PACKET DATA BYTE 0 (PK_AVI_0BYTE) (0x8713)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_0BYTE	7:0	X	861B AVI_info packet Data byte 0 (= checksum)

7.9.5.20 AVI INFO PACKET DATA BYTE *n* (PK_AVI_*n*BYTE (0x8714 – 0x8723)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_*n*BYTE	7:0	X	861B AVI_info packet Data byte *n*

7.9.5.21 AUD INFO PACKET HEADER BYTE 0 (PK_AUD_0HEAD) (0x8730)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_0HEAD	7:0	X	861B AUD_info packet Header byte 0 (= type)

7.9.5.22 AUD INFO PACKET HEADER BYTE 1 (PK_AUD_1HEAD) (0x8731)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_1HEAD	7:0	X	861B AUD_info packet Header byte 1 (= version)

7.9.5.23 AUD INFO PACKET HEADER BYTE 2 (PK_AUD_2HEAD) (0x8732)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_2HEAD	7:0	X	861B AUD_info packet Header byte 2 (= data length)

7.9.5.24 AUD INFO PACKET DATA BYTE 0 (PK_AUD_0BYTE) (0x8733)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_0BYTE	7:0	X	861B AUD_info packet Data byte 0 (= checksum)

7.9.5.25 AUD INFO PACKET DATA BYTE *n* (PK_AUD_*n*BYTE) (0x8734 – 0x8738)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_*n*BYTE	7:0	X	861B AUD_info packet Data byte *n*

7.9.5.26 AUD INFO PACKET DATA BYTE *n* (PK_AUD_*n*BYTE) (0x8739 – 0x873d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_*n*BYTE	7:0	X	861B AUD_info packet Data byte *n* (Reserved for standards extension)

7.9.5.27 MS INFO PACKET HEADER BYTE 0 (PK_MS_0HEAD) (0x8740)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_0HEAD	7:0	X	861B MS_info packet Header byte 0 (= type)

7.9.5.28 MS INFO PACKET HEADER BYTE 1 (PK_MS_1HEAD) (0x8741)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_1HEAD	7:0	X	861B MS_info packet Header byte 1 (= version)

7.9.5.29 MS INFO PACKET HEADER BYTE 2 (PK_MS_2HEAD) (0x8742)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_2HEAD	7:0	X	861B MS_info packet Header byte 2 (= data length)

7.9.5.30 MS INFO PACKET DATA BYTE 0 (PK_MS_0BYTE) (0x8743)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_0BYTE	7:0	X	861B MS_info packet Data byte 0 (= checksum)

7.9.5.31 MS INFO PACKET DATA BYTE *n* (PK_MS_*n*BYTE) (0x8744 – 0x874d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_*n*BYTE	7:0	X	861B MS_info packet Data byte *n*

7.9.5.32 SPD INFO PACKET HEADER BYTE 0 (PK_SPD_0HEAD) (0x8750)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_0HEAD	7:0	X	861B SPD_info packet Header byte 0 (= type)

7.9.5.33 SPD INFO PACKET HEADER BYTE 1 (PK_SPD_1HEAD) (0x8751)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_1HEAD	7:0	X	861B SPD_info packet Header byte 1 (= version)

7.9.5.34 SPD INFO PACKET HEADER BYTE 2 (PK_SPD_2HEAD) (0x8752)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_2HEAD	7:0	X	861B SPD_info packet Header byte 2 (= data length)

7.9.5.35 SPD INFO PACKET DATA BYTE 0 (PK_SPD_0BYTE) (0x8753)

Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	SPD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_0BYTE	7:0	X	861B SPD_info packet Data byte 0 (= checksum)

7.9.5.36 SPD INFO PACKET DATA BYTE *n* (PK_SPD_*n*BYTE) (0x8754 – 0x876e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_*n*BYTE	7:0	X	861B SPD_info packet Data byte *n*

7.9.5.37 VS INFO PACKET HEADER BYTE 0 (PK_VS_0HEAD) (0x8770)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_0HEAD	7:0	X	861B VS_info packet Header byte 0 (= type)

7.9.5.38 VS INFO PACKET HEADER BYTE 1 (PK_VS_1HEAD) (0x8771)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_1HEAD	7:0	X	861B VS_info packet Header byte 1 (= version)

7.9.5.39 VS INFO PACKET HEADER BYTE 2 (PK_VS_2HEAD) (0x8772)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_2HEAD	7:0	X	861B VS_info packet Header byte 2 (= data length)

7.9.5.40 VS INFO PACKET DATA BYTE 0 (PK_VS_0BYTE) (0x8773)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_0BYTE	7:0	X	861B VS_info packet Data byte 0 (= checksum)

7.9.5.41 VS INFO PACKET DATA BYTE *n* (PK_VS_*n*BYTE (0x8773 – 0x878e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_*n*BYTE	7:0	X	861B VS_info packet Data byte *n*

7.9.5.42 ACP INFO PACKET HEADER BYTE 0 (PK_ACP_0HEAD) (0x8790)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_0HEAD	7:0	X	861B ACP_info packet Header byte 0 (= type)

7.9.5.43 ACP INFO PACKET HEADER BYTE 1 (PK_ACP_1HEAD) (0x8791)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_1HEAD	7:0	X	861B ACP_info packet Header byte 1 (= version)

7.9.5.44 ACP INFO PACKET HEADER BYTE 2 (PK_ACP_2HEAD) (0x8792)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_2HEAD	7:0	X	861B ACP_info packet Header byte 2 (= data length)

7.9.5.45 ACP INFO PACKET DATA BYTE 0 (PK_ACP_0BYTE) (0x8793)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_0BYTE	7:0	X	861B ACP_info packet Data byte 0 (= checksum)

7.9.5.46 ACP INFO PACKET DATA BYTE *n* (PK_ACP_*n*BYTE) (0x8794 – 0x87ae)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_*n*BYTE							

Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_*n*BYTE	7:0	X	861B ACP_info packet Data byte *n*

7.9.5.47 ISRC1 INFO PACKET HEADER BYTE 0 (PK_ISRC1_0HEAD) (0x87b0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_0HEAD	7:0	X	861B ISRC1_info packet Header byte 0 (= type)

7.9.5.48 ISRC1 INFO PACKET HEADER BYTE 1 (PK_ISRC1_1HEAD) (0x87b1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_1HEAD	7:0	X	861B ISRC1_info packet Header byte 1 (= version)

7.9.5.49 ISRC1 INFO PACKET HEADER BYTE 2 (PK_ISRC1_2HEAD) (0x87b2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_2HEAD	7:0	X	861B ISRC1_info packet Header byte 2 (= data length)

7.9.5.50 ISRC1 INFO PACKET DATA BYTE 0 (PK_ISRC1_0BYTE) (0x87b3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_0BYTE	7:0	X	861B ISRC1_info packet Data byte 0 (= checksum)

7.9.5.51 ISRC1 INFO PACKET DATA BYTE *n* (PK_ISRC1_*n*BYTE) (0x87b4 – 0x87c2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_*n*BYTE	7:0	X	861B ISRC1_info packet Data byte *n*

7.9.5.52 ISRC2 INFO PACKET HEADER BYTE 0 (PK_ISRC2_0HEAD) (0x87d0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_0HEAD	7:0	X	861B ISRC2_info packet Header byte 0 (= type)

7.9.5.53 ISRC2 INFO PACKET HEADER BYTE 1 (PK_ISRC2_1HEAD) (0x87d1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_1HEAD	7:0	X	861B ISRC2_info packet Header byte 1 (= version)

7.9.5.54 ISRC2 INFO PACKET HEADER BYTE 2 (PK_ISRC2_2HEAD) (0x87d2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_2HEAD	7:0	X	861B ISRC2_info packet Header byte 2 (= data length)

7.9.5.55 ISRC2 INFO PACKET DATA BYTE 0 (PK_ISRC2_0BYTE) (0x87d3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_0BYTE	7:0	X	861B ISRC2_info packet Data byte 0 (= checksum)

7.9.5.56 ISRC2 INFO PACKET DATA BYTE *n* (PK_ISRC2_*n*BYTE) (0x87d4 – 0x87ee)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_*n*BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_*n*BYTE	7:0	X	861B ISRC2_info packet Data byte *n*

7.9.6 HDMI Rx HDCP Registers

Only few registers are listed here. Others can be referred to in HDCP spec. So for the registers 0x88_00 to 0x88_92, please refer to HDCP register 0x00 to 0x92. For example: For register 0x88_08 ➔ Refer HDCP Register 0x08 which is Ri'0 Data.

7.9.6.1 HDCP BCAPS Register (BCAPS) (0x8840)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HDMI_RSVD	Repeater	Ready	FastI2C	Reserved		1.1Fea	Fast_ReAu
Type	RW	RW	RW	RW	RO		RW	RW
Default	0	0	0	0	0		0	0

Register Field	Bit	Default	Description
HDMI_RESERVED	7	0	0: automatic move to HDMI mode is not performed.
REPETER	6	0	1: HDCP Repeter
READY	5	0	KSVFiFo is Ready for 2nd Authentication
FAST(DDC I2C speed)	4	0	1: 400 KHz Supported
Reserved	[3:2]	0	
1.1_FEATURES	1	0	Fixed at '0'
FAST_REAUTH	0	0	Fast re-authentication

7.9.6.2 HDCP Rx BSTAUS0 Register (BSTATUS0) (0x8841)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MAX_DEVS_EXCEEDED	DEVICE_COUNT						
Type	RW	RW						
Default	0	0x00						

Register Field	Bit	Description
MAX_DEVS_EXCEEDED	7	If later stage connection devices number is 17 or more, set to "1".
DEVICE_COUNT	[6:0]	Later stage connection device number (not including self)

7.9.6.3 HDCP Rx BSTAUS1 Register (BSTATUS1) (0x8842)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		HDMI_RSVD	HDMI_MODE	MAX_EXCED	DEPTH		
Type	RO		RW	RW	RW	RW		
Default	0		0	0	0	0		

Register Field	Bit	Default	Description
Reserved	[7:6]	0	
HDMI_RSVD	5	0	V' value calculation state machine reset 1: Reset (Auto clear)
HDMI_MODE	4	0	HDMI mode setting 0: DVI mode, 1: HDMI mode
MAX_EXCED	3	0	Topology error indicator. When set to one, more than seven levels of the repeater have been cascaded together.
DEPTH	[2:0]	0	Three-bit repeater cascade depth. This value gives the number of attached levels through the connection topology.

7.9.6.4 KSVFIFO Register (KSVFIFO) (0x8843)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	KSVFIFO							
Type	RW							
Default	0							

Register Field	Bit	Default	Description
KSVFIFO	[7:0]	0x00	Total 80Byte for 16Devices, DDC Address: 0x74, Offset 0x43

8 Package

TC358749 Package (80-pin, P-VFBGA80-0707-0.65-001)

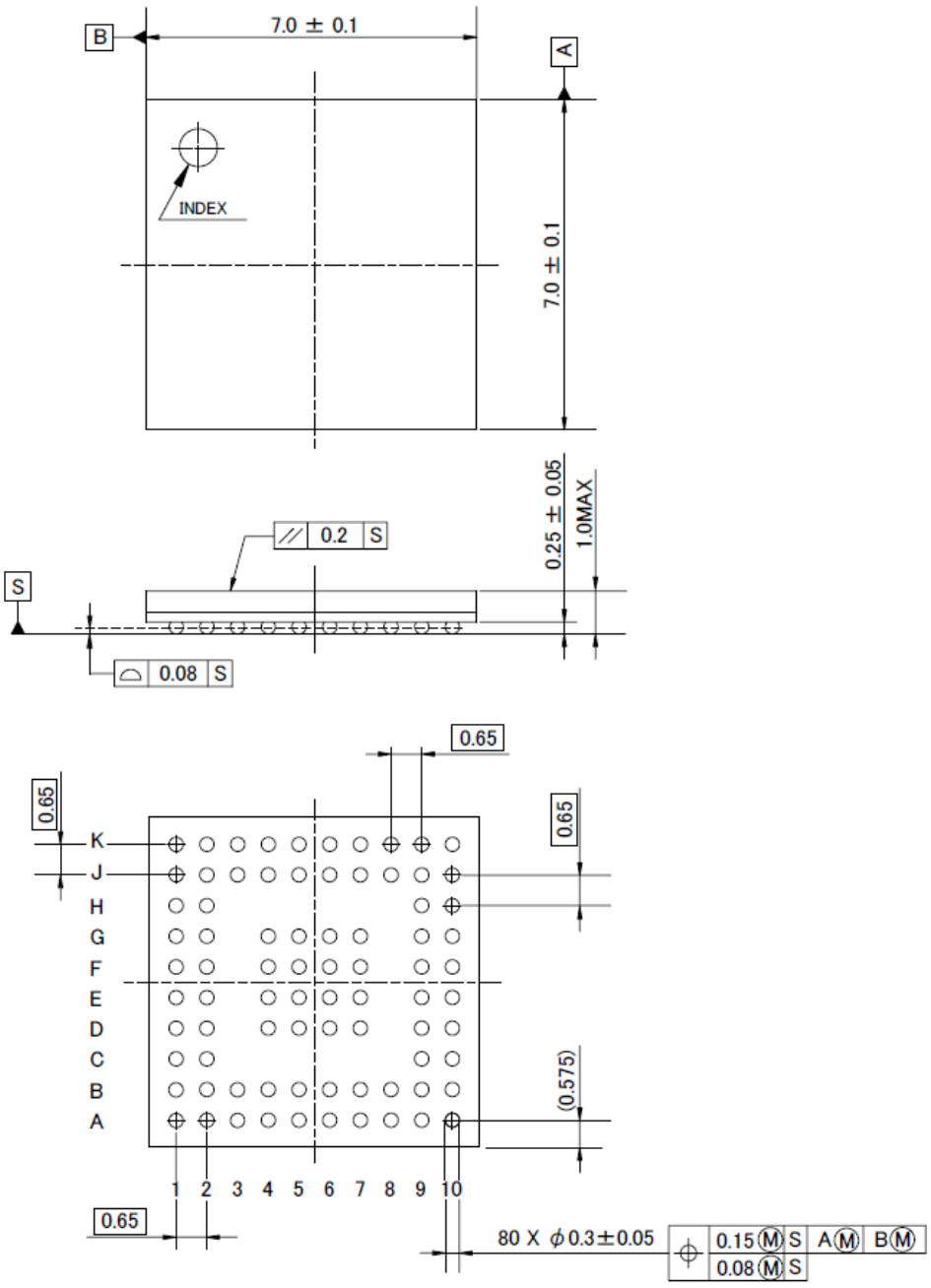


Table 8-1 Mechanical Dimension for TC358749

Dimension	Min.	Typ.	Max.
Solder ball pitch	---	0.65 mm	---
Package dimension	---	7.0 x 7.0 mm^2	---
Package height	---	---	1.0 mm

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

VSS= 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	-0.3 ~ +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 ~ +1.8	V
Supply voltage (1.2V – MIPI CSI-2 PHY)	VDD_MIPI	-0.3 ~ +1.8	V
Supply voltage (3.3V – HDMIRX Phy)	AVDD33	-0.3 ~ +3.9	V
Supply voltage (1.2V – HDMIRX Phy)	AVDD12	-0.3 ~ +1.8	V
Input voltage (CSI-2 IO)	V_{IN_CSI-2}	-0.3 ~ VDD_MIPI+0.3	V
Output voltage (CSI-2 IO)	V_{OUT_CSI-2}	-0.3 ~ VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 ~ VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 ~ VDDIO+0.3	V
Juntion temperature	Tj (TBD)	TBD to ~125	^{o}C
Storage temperature	Tstg	-40 ~ +125	^{o}C

9.2 Recommended Operating Condition

VSS= 0V reference

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (1.8/3.3V – Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3V – HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (3.3V – HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply voltage (1.2V – HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply voltage (1.2V – MIPI CSI-2 PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	Ta (TBD)	-30	+25	+70	^{o}C
Supply Noise Voltage	V_{SN}			100	mV_{pp}

9.3 DC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit

Input voltage, High level input Note1	V_{IH}	0.7 VDDIO		VDDIO	V
Input voltage, Low level input Note1	V_{IL}	0		0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note1,2	V_{IHS}	0.7 VDDIO		VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note1,2	V_{ILS}	0		0.3 VDDIO	V
Output voltage High level Note1, Note2	V_{OH}	0.8 VDDIO		VDDIO	V
Output voltage Low level Note1, Note2	V_{OL}	0		0.2 VDDIO	V
Input leak current, High level (Condition: V_{IN} = +VDDIO, VDDIO = 3.6V)	I_{ILH1} (Note4)	-10	-	10	uA
Input leak current, Low level (Condition: V_{IN} = 0V, VDDIO = 3.6V)	I_{ILL1} (Note5)	-10	-	10	uA

Note1 : Each power source is operating within recommended operation condition.

Note2 : Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4 : Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note5 : Normal pin applied VSS (0V) to Vin (input voltage)

10 Timing Definitions

10.1 RefClk Input Requirement

Parameter	Min.	Typ.	Max.	Unit
Frequency		26/27 or 42		MHz
Duty Cycle	40	50	60	%
Jitter	-100	0	100	ppm

10.2 MIPI CSI-2 Timings

Timing specification below has been ported from Draft MIPI Alliance specification for D-PHY version 0.91.00 r0.01. Timing defined in Draft MIPI Alliance specification for D-PHY version 0.91.00 r0.01 has precedence over timing described in the sections below.

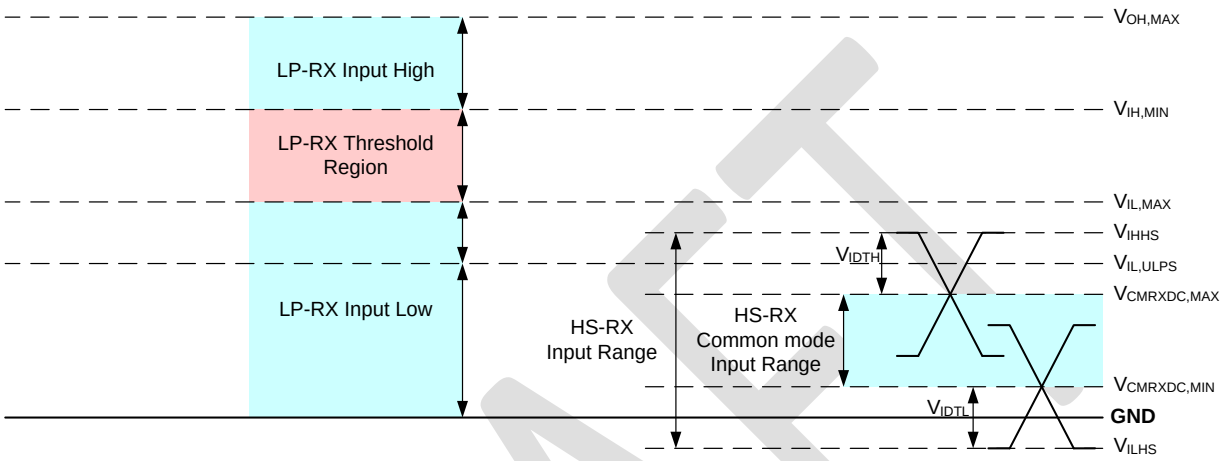


Figure 10-1 Signaling and voltage levels

Table 10-1 DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{PIN}	Pin signal voltage range	-50		1350	mV	
$V_{PIN(absmax)}$	Transient pin voltage	-0.15		1.45	V	
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(absmax)}$ or below $V_{PIN(absmax)}$.			20	ns	3
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
$V_{CMRX(DC)}$	Common-mode voltage HS receiver mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1

V_{ILHS}	Single-ended input low voltage	-40			mV	1

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value included a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.
3. The voltage undershoot or overshoot beyond V_{PIN} is only allowed during a single 20 ns window after any LP-0 LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

Table 10-2 High Speed AC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz- 450MHz	-50		50	mV	1,3

Notes:

1. Excluding `static' ground shift of 50mV
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. Voltage difference compared to the DC average common-mode potential.

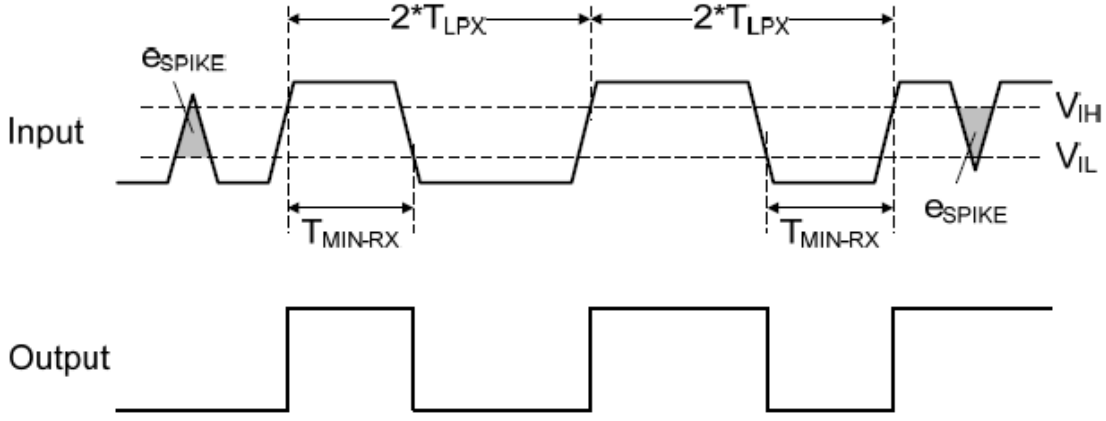


Figure 10-2 Input Glitch Rejection

Table 10-3 Low Power AC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V.ps	1,2,3
T_{MIN-RX}	Minimum pulse width response	20			ns	4

V_{INT}	Peak interference amplitude			200	mV	
F_{INT}	Interference frequency	450			MHz	
T_{LPX}	Length of any Low Power state period	50			ns	

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 or below V_{IH} when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

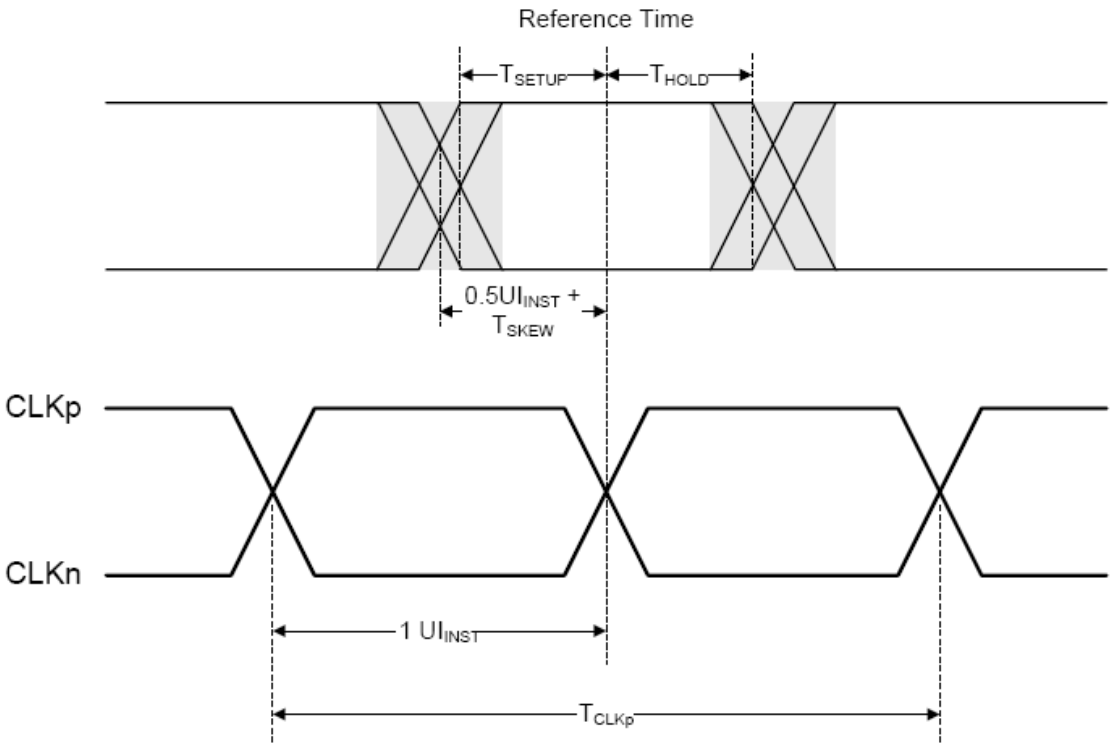


Figure 10-3 Data to clock timing reference

Table 10-4 Data-Clock timing specification

Parameter	Description	Min	Nom	Max	Units	Notes
T_{SKEW}	Data to clock skew measured at the transmitter	-0.15		0.15	UI_{INST}	
T_{SETUP}	Data to clock setup time at	0.15			UI_{INST}	

	receiver					
T_{HOLD}	clock to data hold time at receiver	0.15			UI_{INST}	
UI_{INST}	1 Data bit time (instantaneous)			12.5	ns	
T_{CLKp}	Period of dual data rate clock	2	2	2	UI_{INST}	

10.3 I2C Timings

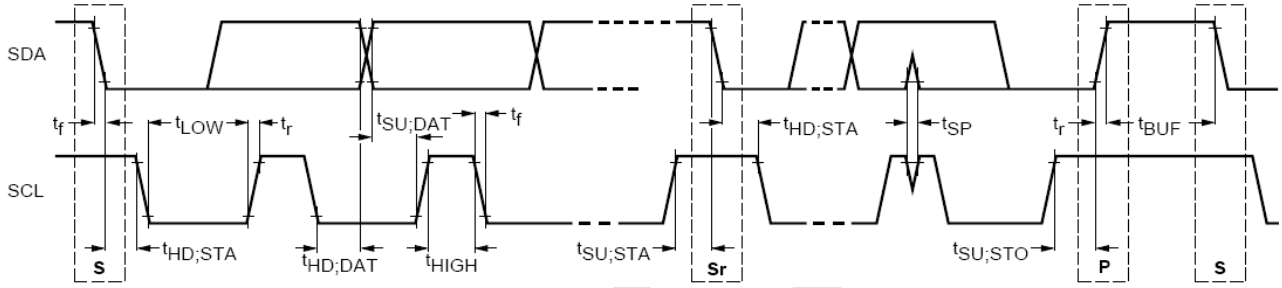


Figure 10-4 I2C Timing Diagram

Table 10-5 I2C timing specification

Item	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	2	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	µs
Data hold time: for I2C-bus devices	$t_{HD;DAT}$	0	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1Cb	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	µs

Note: Cb = Capacitive load for each bus line (400pF max.)

10.4 HDMI-RX Input

(Ta=25℃,AVDD12VADC =1.25V, DVDD12HDMI =1.20V, AVDD33VADC =3.3V, AVDD33VADC=3.3V, DVDD33HDMI=3.3V)

Parameter	Symbol	min	typ	max	unit	Comment
ADC Input Level	VIN	---	0.7	0.8	Vp-p	SH_GAIN=1 (x1.0 mode)
ADC Differential Error	EDNL1	-2	---	2	LSB	Clock Frequency: 54 MHz, 162 MHz
ADC Integration Error	EINL1	-2.5	---	2.5	LSB	Clock Frequency: 54 MHz, 162 MHz
ADC Max Clock Frequency	FMAX_1	10	54	60	MHz	ADC A-ch
	FMAX_2	10	---	165	MHz	ADC B-ch, C-ch, D-ch
DAC Output Impedence	Zy	160	200	240	Ω	
HDMI Clock Frequency	FIN	25	---	225	MHz	300 mVpp
HDMI minimum Amplitude	VMIN	159	---	---	mVp-p	225MHz at TP2 Compliance test (TestID 8-5)

10.5 I2S/TDM Timings

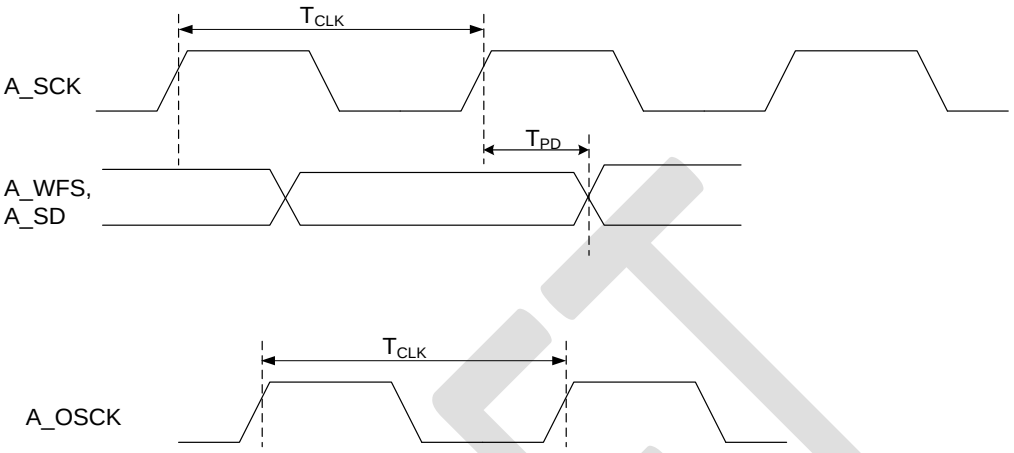


Figure 10-5 I2S/TDM Timing Diagram

Table 10-6 I2S/TDM timing specification

Item	Symbol	Min	TYP	Max	Unit
Propagation Output Delay	T_{PD}	0	--	9	ns
Clock Period	T_{CLK}	20	--	--	ns

Notes: Above timing are for 15pf load on all I2S/TDM signals

10.6 SLIMbus IO

10.6.1 Clock Output Timing

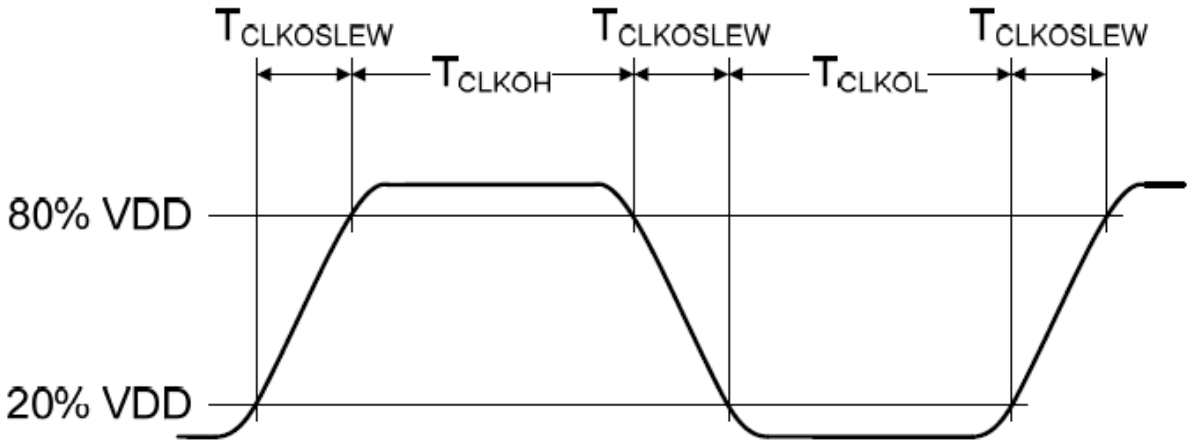


Figure 10-6 Clock Driver Output Waveform Constraints

Table 10-7 Clock Output Timing Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Clock Output High Time	T_{CLKOH}		12	--	--	ns
Clock Output Low Time	T_{CLKOL}		12	--	--	ns
Clock Output Slew Rate	SR_{CLK}	20%<VO<80%	0.02*VDD	--	0.2*VDD	V/ns

10.6.2 Clock Input Timing

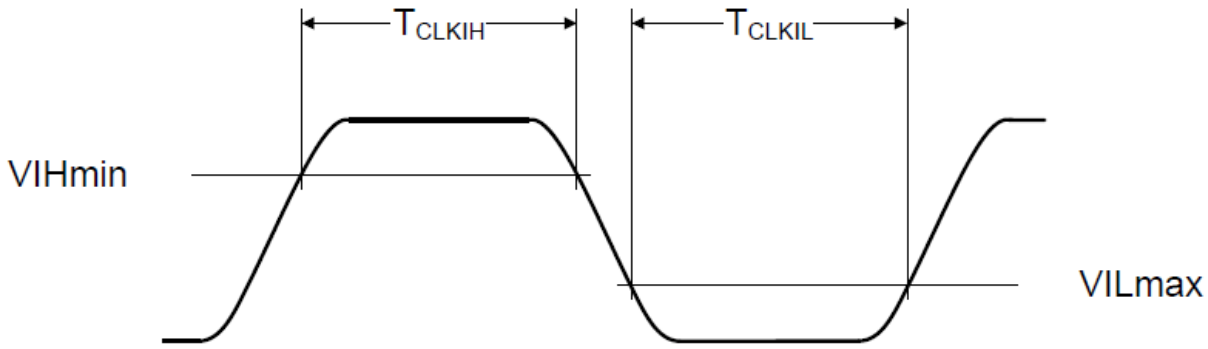


Figure 10-7 Received Clock Signal Constraints

Table 10-8 Clock Input Timing Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Clock Input High Time	T_{CLKIH}		12	--	--	ns
Clock Input Low Time	T_{CLKIL}		12	--	--	ns
Clock Input Slew Rate	SR_{CLKI}	20%<VI<80%	0.02*VDD	--	--	V/ns

Table 10-9 Clock Input Electrical Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Clock Input Hysteresis	H_{CLKI}		50	--	--	mV

10.6.3 Data Timing

Table 10-10 Data Output Timing Characteristics

Item	Symbol	Condition	Min	TYP	Max	Unit
Data Output Slew Rate	SR_{DATA}	20%<VO<80%	--	--	0.5*VDD	V/ns
Time for Data Output Valid	T_{DV}		--	--	12	ns

Table 10-11 Data input Timing Requirements

Item	Symbol	Condition	Min	TYP	Max	Unit
Data Input Hold Time	T_H		2	--	--	mV
Data Input Setup Time	T_{SETUP}		3.5	--	--	mV

Table 10-12 Driver Disable Timing Specification

Item	Symbol	Condition	Min	TYP	Max	Unit
Driver Disable Time	T_{DD}		--	--	10	ns

Table 10-13 Bus Holder Electrical Specification

Item	Symbol	Condition	Min	TYP	Max	Unit
Bus Holder Output Impedance	R_{DATAS}	0.1*VDD<V<0.9*VDD	10K	--	50K	Ohm

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